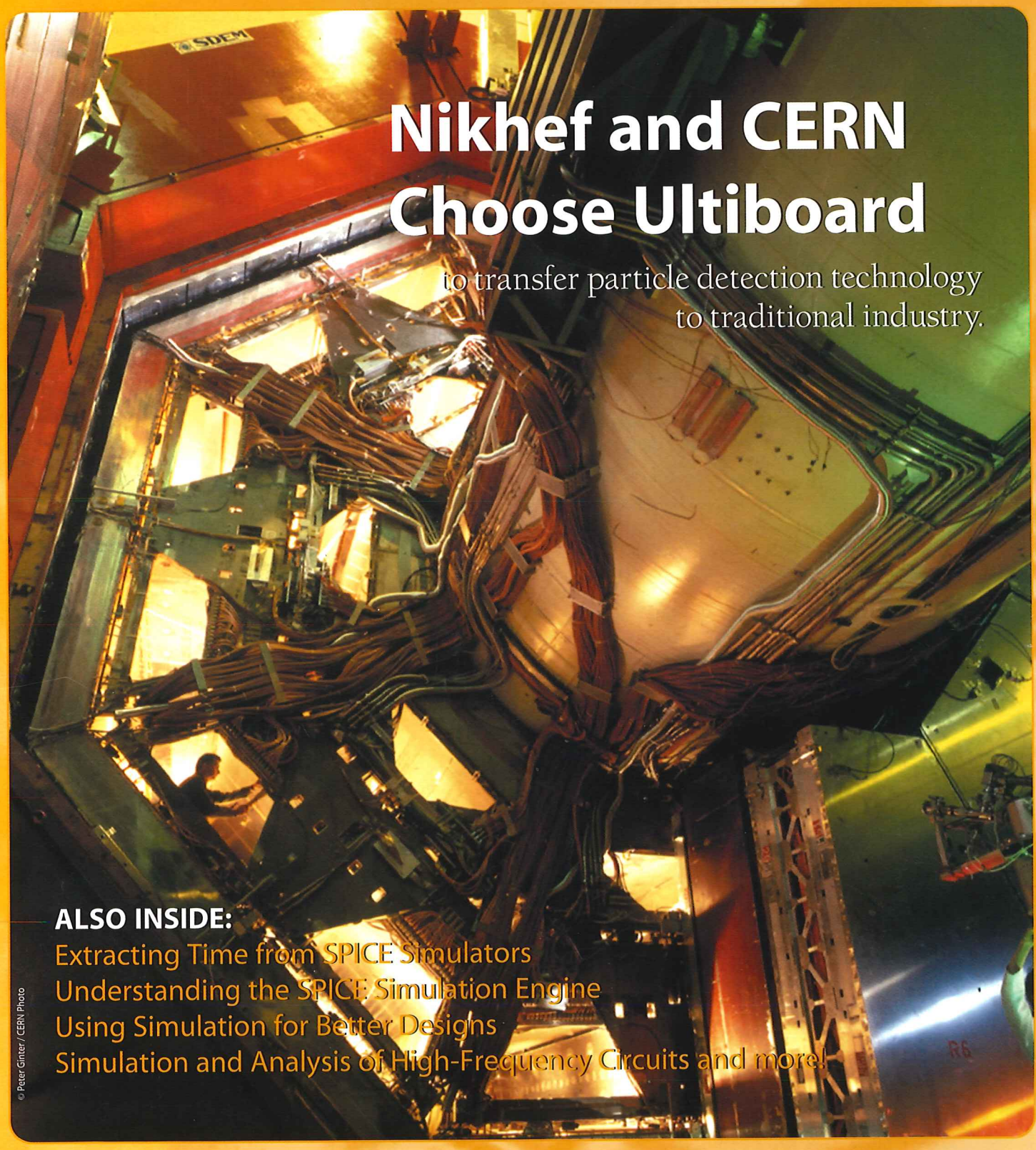
designSOLUTIONS

Practical Information to Solve Circuit Design Challenges

ISSUE 1, 2003



Nikhef and CERN Choose Ultiboard

to transfer particle detection technology to traditional industry.

ALSO INSIDE:

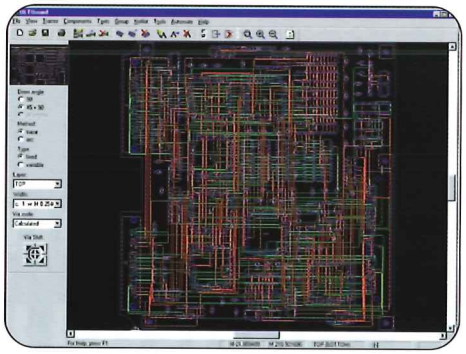
Extracting Time from SPICE Simulators
Understanding the SPICE Simulation Engine
Using Simulation for Better Designs
Simulation and Analysis of High-Frequency Circuits and more!

News

ACQUISITION OF KEY AUTOPLACEMENT AND AUTOROUTING TECHNOLOGY

Electronics Workbench has acquired key autoplacement and autorouting technology from Bartels System GmbH, in Germany. This code which made up the Ultiroute autorouter, was previously licensed to Electronics Workbench under an OEM arrangement. Acquiring complete rights to this intellectual property meets a number of objectives for Electronics Workbench. Firstly, it enables the firm to control the development of the code and ensure important functionality improvements and additions to the product well into the future. The acquisition will also lead the way for tighter integration of the autorouting and autoplacement technology within Ultiboard. The acquired technology is unique in the industry by combining both grid-based and shape-based routing in a single product. In addition, the advanced autoplacement technology has already earned great respect from the many thousands of Electronics Workbench professional customers. Internal Electronics Workbench benchmark studies show this technology consistently performs to a standard of speed, accuracy and manufacturability that is more commonly associated with enterprise-wide solutions.

Commenting on the acquisition, Bill Wignall, president and CEO of Electronics Workbench said, "We need full control over the future direction of R&D to drive our integration strategy. The logical way to do this is through ownership of key IP. We have built a successful business model around the principles of licensing IP, confirming the viability of a product line for us, and then acquiring full rights to further develop it into our line of professional EDA products." Wignall added, "Our customers want integrated solutions because moving from application to application



costs time and money when designing today's PCBs. These application discontinuities hinder a fluid design methodology that can only be created by a fully integrated solution."

ELECTRONICS WORKBENCH TAPS INDUSTRY TALENT AS NEW VP OF SALES AND MARKETING

Bill Wignall, CEO of Electronics Workbench announced the appointment of Mr. Ian Suttie, P.Eng. to the position of Vice President of Sales and Marketing. Suttie will be instrumental in developing the sales and marketing strategies that will support the company's continued growth in the professional PCB design market.

Suttie brings 15 years of experience in sales, marketing and executive management to his new position. In addition to his direct management experience, he has also served as a director of several private companies, industry associations and standards organizations.

MULTISIM AND ULTIBOARD SERVICE PACK 2 AVAILABLE

Service Pack 2 is now available for both Multisim and Ultiboard. If you do not yet have these most up-to-date releases, please contact your sales representative. The Service Pack 2 changes include fixes to commonly encountered bugs as well as new functionality requested by users. Significant changes to Multisim include over 400 new symbols, optimization of existing models for higher accuracy, as well as improvements to the Orcad import. The Ultiboard Service Pack 2 includes significant improvements to the Gerber 274x export and delivers the ability to import Orcad or Eagle files.

WEB PATCHES AVAILABLE

Software patches are periodically posted on the Electronics Workbench websites. These releases usually include only small fixes, in contrast to a Service Pack that contains a larger number of fixes and usually new functionality as well. Be sure to visit our website regularly to keep your software as up-to-date as possible.

http://www.electronicsworkbench.com
http://www.ewbeurope.com

UK CUSTOMERS HANDLED BY ELECTRONICS WORKBENCH DIRECTLY

As of September 1st, 2002, sales and support for Electronics Workbench products in the United Kingdom are being handled directly by Electronics Workbench Europe. Electronics Workbench is now 20 years old and its products have gone through 6 major generational releases. Because the product technology has become so technically advanced and due to the demands of growth in this market, UK customers will now be served by the dedicated technical support and customer service from Electronic Workbench's European headquarters. UK customers can contact Electronics Workbench Europe at:

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Fax: +44-(0)2072876777
Web: www.electronicsworkbench.co.uk
Mail: 211 Piccadilly, London,
The United Kingdom, W1J 9HF

Events

EXHIBITIONS

DESIGN AUTOMATION & EMBEDDED SYSTEMS – EINDHOVEN NOVEMBER 2002

In November 2002, Electronics Workbench presented at the D & E show in Eindhoven, The Netherlands.

ELECTRONICA – MUNICH NOVEMBER 2002

Electronics Workbench demonstrated at Electronica during November 2002. We thank the more than 1,000 people who visited our stand at Messe München in Germany.

PCB WEST – SAN JOSE, CA MARCH 2003

Electronics Workbench will exhibit at PCB West in San Jose, CA in March 2003. If you would like a free entrance pass, please contact your Account Manager to arrange one for you. If you plan to attend, please stop by the booth and find out about the latest products available.

PCB DESIGN CONFERENCE WEST

TECHNOLOGY ROADSHOWS

MARCH & APRIL 2003

During March and April 2003, Electronics Workbench will be conducting information seminars at the following locations and dates:

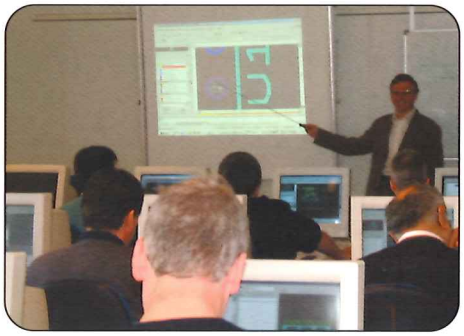
Gent, Belgium	February 25
Eindhoven, The Netherlands	February 27
Apeldoorn, The Netherlands	March 4
Leiden, The Netherlands	March 6
Reading, United Kingdom	March 10
Bristol, United Kingdom	March 11
Birmingham, United Kingdom	March 12
Manchester, United Kingdom	March 13
Edinburgh, United Kingdom	March 14
Paris, France	March 27
Frankfurt, Germany	April 7
Zurich, Switzerland	April 8
Vienna, Austria	April 9
Munich, Germany	April 10

These FREE roadshow presentations will focus on demonstrating the techniques over 150,000 customers use to save time, save money, and build better circuits. They are intended for people who do not yet own Multisim or Ultiboard. Space is limited, so please contact your Account Manager to reserve a place for you.

TRAINING

San Jose, California – Multisim – March 17-18
San Jose, California – Ultiboard – March 19-20
Naarden, The Netherlands – Multisim – May 6-7
Naarden, The Netherlands – Ultiboard – May 20-21
Raleigh, North Carolina – Multisim – May 20-21
Raleigh, North Carolina – Ultiboard – May 22-23

For a course description, dates and locations, please visit www.electronicsworkbench.com or www.ewbeurope.com



CONTENTS

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This publication has been produced by Electronics Workbench, a world leader in circuit design software for the mainstream professional electronics designer.

Design Solutions is available free of charge to qualified electronics engineers, designers and those within the EDA industry. All advertising requests and reader enquires should be sent to our Canadian office at: Electronics Workbench, 111 Peter Street, Suite 801, Toronto, Ontario, Canada M5V 2H1.

Extracting Time from SPICE Simulators

SPICE may not output time values, but there are ways to get the data you want.

By Alexander Ehle

Modeling time dependent functions in SPICE simulators is not a straightforward task since time is not a variable made available to users for analysis. This article will illustrate a simple technique for extracting time from a runtime simulation. It will also describe some applications of this method and provide some practical tips when performing time extraction.

SPICE outputs voltage values, not time values. In order to extract time values from the SPICE netlist during simulation, time values must be translated into some equivalent voltage value which can then be processed or analyzed. Most simulators do not provide any standard devices to perform this operation. But with a simple trick, a transient analysis can be used to extract simulation time.

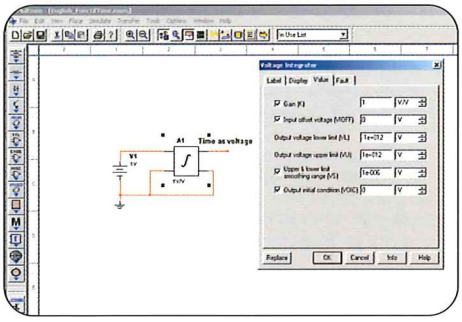


Figure 1 - Integration circuit to represent transpired time as a voltage.

In order to establish a one-to-one translation between time and voltage, feed a 1V signal into an integrator that has a 1V/sec integration value. Figure 1 shows such a circuit configuration in Multisim. The integrator block is an XSPICE model from the Multisim library. The model definition for this device is shown in Figure 2. If the simulator does not support XSPICE models, or if you simply want to make your own integrator, you can easily create a netlist for an integration device using a resistor, capacitor, and three controlled sources (Figure 3). When simulating integrators, it is generally a good idea to set the start conditions to zero so that the capacitor has no charge. A simple way to accomplish this is to use a pulse generator at the start of the simulation to initialize the circuit. In the SPICE netlist, the controlled source B1 acts as an inverter because the pulse generator V2 has a 1Volt signal at the starting point.

```
.SUBCKT TIME2 1
*
* XSPICE / Multisim
*
V1 2 0 DC 1
AA1 %vd(2 0) %vd(1 0) INTTIME1
.MODEL INTTIME1 INT(GAIN=1
+ IN_OFFSET=0 OUT_LOWER_LIMIT=-1e+012
+ OUT_UPPER_LIMIT=1e+012
+ LIMIT_RANGE=1e-006 OUT_IC=0)
.ENDS
```

Figure 2 - XSPICE model of integrator in Multisim.

```
.SUBCKT TIME1 1
*
* SPICE3F5
*
G1 0 3 2 0 1
R1 0 3 1E+12
C1 0 3 1 IC=0
E1 1 0 3 0 1
B1 2 0 V=u(-V(4,0)+1E-99)
V2 4 0 PULSE(1 0 0 1E-99 1E-99)
.ENDS
```

Figure 3 - SPICE netlist to model general integrator.

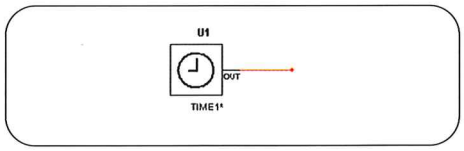


Figure 4 - Symbol to represent Time Extraction subcircuit from Figure 1.

The effect is that at the starting point, a 0V signal is applied to the integrator. After a very short T=1E-99 seconds, the pulse generator shuts off and the original 1 Volt signal will have switched on the integrator for the simulation.

The whole circuit from Figure 1 can be saved in Multisim as a subcircuit. This subcircuit can subsequently be stored in the parts library and assigned a symbol as shown in Figure 4. The symbol to represent the simple time extraction circuit was created using the Multisim symbol editor.

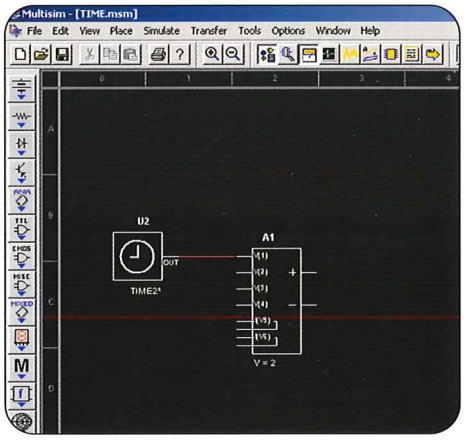


Figure 5 - Nonlinear dependent source being used to generate a sinusoidal source.

To test the subcircuit, a transient analysis has been run for 1 second. Both SPICE models generate similar results, but the XSPICE model (Figure 2) has much less load on the simulator than the SPICE-3 subcircuit model (Figure 3). The result of the transient analysis clearly shows the 1:1 relationship between simulation time and extracted voltage. Wherever we need the time value of the simulation, we can now substitute an equivalent voltage value.

To illustrate a simple application of the Time subcircuit described above, we will demonstrate how to make user-defined signals. Multisim has a nonlinear dependent source that generates voltage or current signals using complex expressions. Expressions may use the following operators:

+ - * / ^ unary-

in combination with the following functions:

abs asin atanh exp sin tan

acos asinh cos ln sinh u

acosh atan cosh log sqrt uramp

$$V = V_p * SIN(2\pi f * V(1))$$

For example, a sinusoidal signal can be generated by entering the above expression into the nonlinear dependent source and feeding it with the output of the time subcircuit V(1) as shown in Figure 5. The amplitude, constant, and the frequency are replaced with their real values. To generate a similar Cosine signal, simply replace the SIN command with a COS command in the nonlinear dependent source. Similarly, by simply changing V= to I= in the nonlinear dependent source, every signal can be generated as a current source. This same basic technique can be extended to many and more complex applications, some of which are described below.

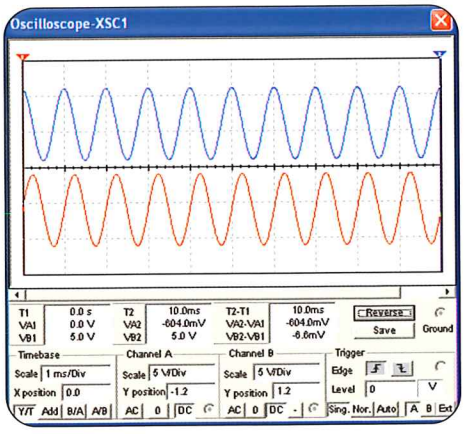


Figure 6 - Multisim oscilloscope showing generated SIN and COS signals.

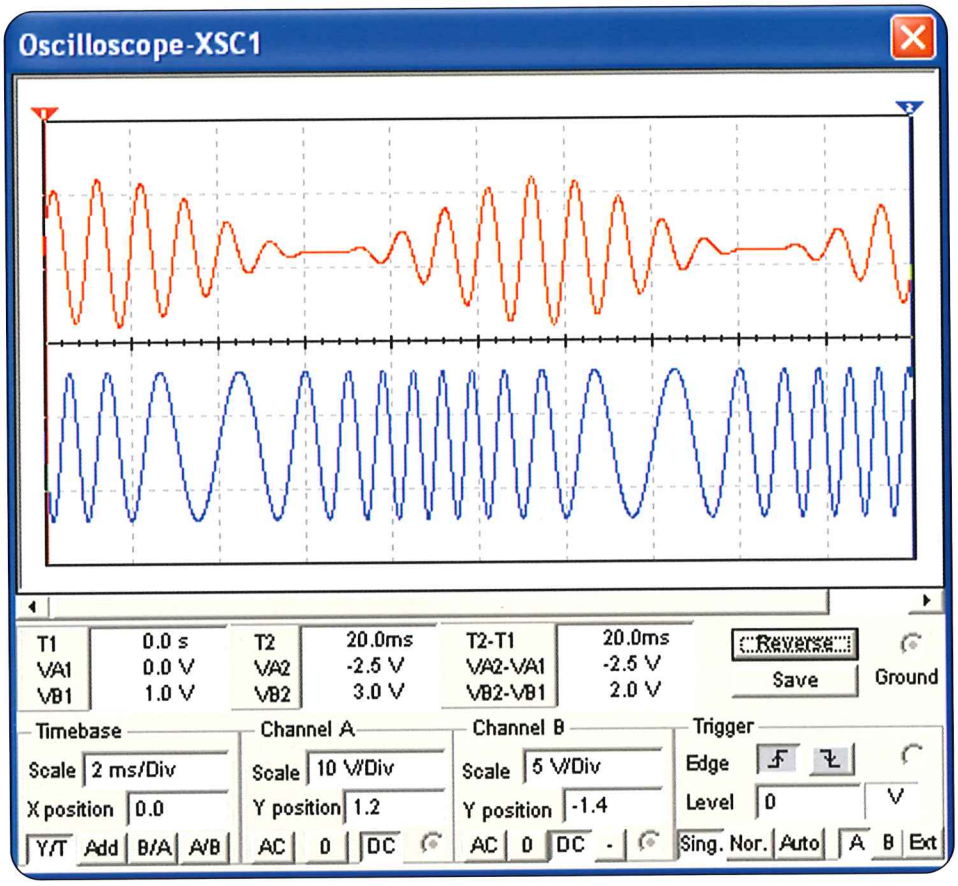


Figure 7 - Multisim oscilloscope showing generated FM and AM signals.

We can introduce some additional variables to our basic SIN functions such as offset and some damping factor loss:

$$V = V_{OFFSET} + V_P * e^{-(V(1)*DF)} * SIN(2\pi f * V(1))$$

Similarly, we can make modifications to basic functions to create frequency modulated and amplitude modulated signal sources (Figure 7):

$$V = V_P * SIN(2\pi f_{CARRIER} * V(1) + m * SIN(2\pi f_{MOD} * V(1)))$$

$$V = Vc * SIN(2\pi f_{CARRIER} * V(1)) * (1 + m * SIN(2 * \pi * f_{MOD} V(1))))$$

A square wave signal can be derived from a basic sine wave signal. By using the u-function in the nonlinear dependent source, a zero-cross detector is implemented. In essence, this u-function serves as a simple switch, triggered by values greater than or equal to zero:

$$V = V_P * u(1 * SIN(2\pi f * V(1))) - V_{OFFSET}$$

While all the above signals are also available as standard sources in the Multisim simulator, a tone burst signal is not. Tone burst signals are used principally in audio measurement technology. They are used to transmit sinusoidal bursts into a circuit or as basic step signals. A typical application would be to measure the transient response of speakers, filters, or equalizers. Tone burst signals are also used to measure the dynamic response of peak limiters or time delays in electronic delay devices. The basic operation of a tone burst generator is to transmit sinusoidal bursts over a period of time.

A tone burst signal can be made by forcing pauses and delays onto a SIN generator. A simple pulse source can be used to control the SIN source. The settings for the pulse source are calculated taking into consideration the SIN signal's frequency as well as the desired number of periods for the pulses and pauses:

$$T_{BURST} = \frac{\#BURSTPERIODS}{f}$$

$$T_{PAUSE} = \frac{\#PAUSEPERIODS}{f}$$

$$T_{BURST} = T_{BURST} + T_{PAUSE}$$

As an example, selecting a 1kHz signal with an impulse time of 3 msec and a period of 5 msec will result in a burst of three sine cycles, and then two off sine cycles (Figure 8).

Time extraction can also be put to interesting use in time dependent switch functions. Because time signals are available as equivalent voltage values, thy can be operated upon using voltage controlled switches. In this manner, input and output timepoints can be set using input and output voltages. Figure 9 shows the generation of a pulse with a period of exactly 1 msec. The pulse turns off when the voltage output of the Time Subcircuit reaches 1 mV.

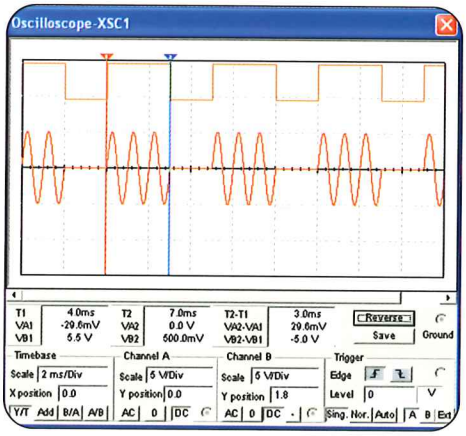


Figure 9 - Tone burst signal with 3 on-cycles followed by 2 off-cycles.

A further application of this time extraction technique is simulating the ageing process of components. Age dependent deviations in a device's output voltage can be modeled as a time dependent offset voltage The potential uses of this time extraction technique is limited only by your imagination.

```
.SUBCKT TONEBURST 1 2
* 1 = TIME
* 2 = OUT
*
B1 2 0 V=(AMPLIITUDE*SIN(2*3.141*FREQ*V(1)))*V(3)
V1 3 0 PULSE(0 1 0 1E-9 1E-9 TBURST TPERIODE)
.ENDS
```

Figure 8 - Toneburst netlist.

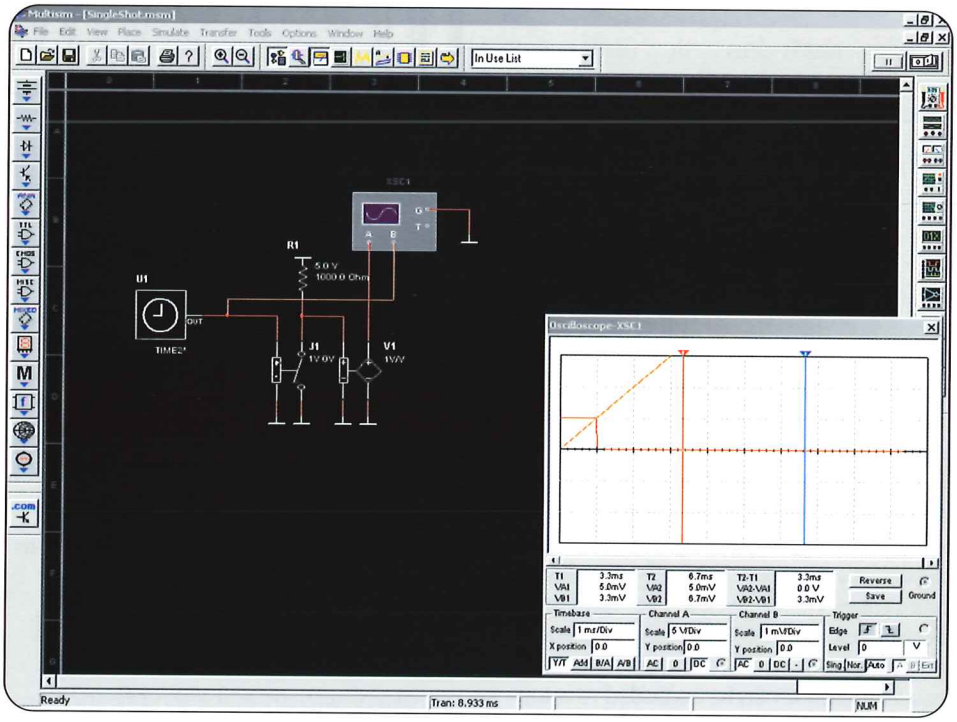


Figure 10 - Time dependent switch circuit.

Literature:

- Multisim 2001 User Guide, Interactive Image Technologies Ltd.
- XSPICE Software User's Manual, December 1992, Georgia Tech Research Institute, Atlanta
- SPICE3F5 User Manual, University of Berkeley, California

Using the Multisim Oscilloscope

Multisim's oscilloscope offers all real world features and more.

By Dan Harris & Janina Dziejko

Multisim's oscilloscope is a very powerful, yet easy-to-use analysis tool. In addition to offering all real world capabilities, it offers some features simply not available with real scopes. This article will describe some techniques to get the most out of Multisim's oscilloscope, and also illustrate some useful features that are possible due to the fact that this virtual instrument calculates and stores results digitally.

All settings on this virtual oscilloscope are similar to those on a real oscilloscope (timebase, input sensitivity, trigger functions, etc.). Two measurement cursors, together with a direct readout display, facilitate analysis of measured results. Once a simulation is activated, the oscilloscope automatically displays the signal waveforms. All oscilloscope settings can be adjusted and changed while a simulation is running.

The refreshed signals are automatically displayed without having to stop and restart the simulation. The only exception occurs if you make significant changes to the oscilloscope's timebase setting to display much more detail in the signals. In addition to controlling the scaling for the horizontal x-axis, the timebase setting is used by the simulation engine to define the sampling rate or timestep value for the SPICE analysis.

Smaller timesteps provide more precision, but also slow down the simulation. If changes to the oscilloscope's timebase setting ever result in irregular or choppy signals, simply turn the simulation button off, and then back on again. Based on the lower timebase value, the simulator will start a new simulation using smaller timesteps. To obtain meaningful simulation results, the timebase setting must be inversely proportional to the frequency of the circuit's function generator or AC source. In other words, the higher a circuit's frequency, the smaller the required timebase — just as with a real oscilloscope. For example, in order to display a period for a 1kHz signal, the timebase should be set to 0.1ms. To display a 10kHz period, the timebase should be set to 0.01ms.

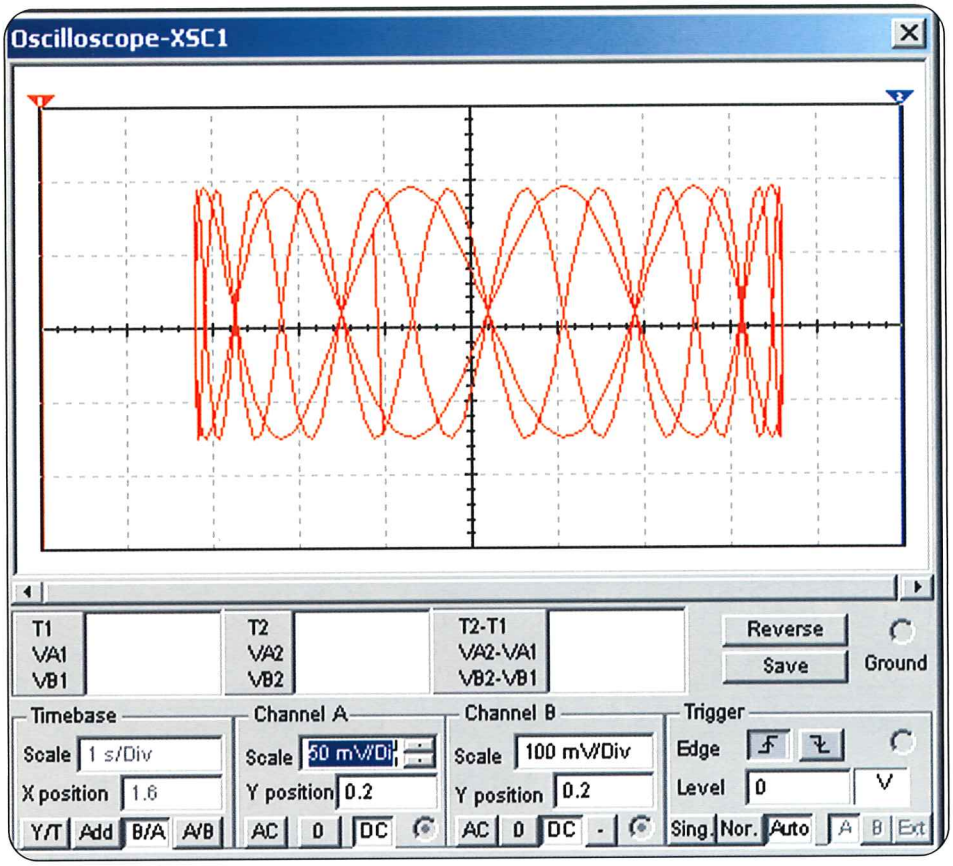


Figure 1 - Lissajous figure displayed using A/B mode.

Just as with a real scope, Multisim's oscilloscope has three different display modes: Y/T, A/B, and B/A. In Y/T, magnitude is displayed against time, and one channel is displayed above the other (A/B or B/A). In A/B or B/A mode, frequency and phase positions (Lissajous figures) or hysteresis loops can be shown.

If the oscilloscope's ground connection is not specifically connected to any point in the circuit, it uses the circuit's ground as a default. So if you are happy with all signals being displayed with reference to the circuit's ground, there is no need to connect the oscilloscope's ground terminal.

The trigger level is the point on the y-axis of the oscilloscope that the signal must pass through in order to trigger capture for the display. Remember that the trigger level will not be crossed in the case of signals whose shapes have no rise or edge. So for edgeless or linear signals, always use the "AUTO" setting for triggering. The "AUTO" setting is also appropriate when signals need to be displayed as quickly as possible.

The Multisim oscilloscope includes a single sweep function. In this "SING." mode,

the scope will display a waveform from the moment its triggering level is reached, until the point that the signal spans the end of the screen on the right. The displayed trace will not change until the "SING." button is pressed again. Because the scope screen is not constantly changing, you can perform accurate measurements on the displayed waveforms. But despite the fact that this mode only shows signal segments, all waveform data is saved in a temporary file. The Multisim oscilloscope has a scroll bar that allows you to move back and forth in time to display the whole signal history. This is an extremely useful capability enabling you, for example, to compare start-up to steady state conditions.

The "NOR." mode will plot waveforms, one screen at a time, until you manually stop the simulation. When the scope has

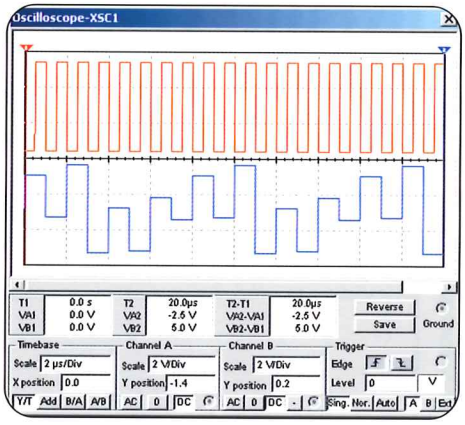


Figure 2 - Displaying a single signal sweep.

plotted a signal to the right edge of the screen, that waveform segment is discarded and the next portion of the waveform is plotted. Unlike the "AUTO" and "SING." modes, the "NOR." mode does save the history of simulation results.

Multisim lets users pause and restart simulation. This gives users the ability to freeze the oscilloscope in time, make measurements, and then resume the simulation to get new data at will.

Because the "AUTO" and "SING." modes store the whole signal's history in a temporary file, the Multisim oscilloscope gives users the option to save that data permanently to file. All waveforms shown on the oscilloscope are also loaded into the program's grapher. The grapher is a multi-purpose display tool to view, adjust, save, and export data. You can use the grapher to customize grids, add titles, and print high quality graphs. From the grapher, a single button launches and loads results into Microsoft® Excel® or Mathsoft's Mathcad® for further analysis.

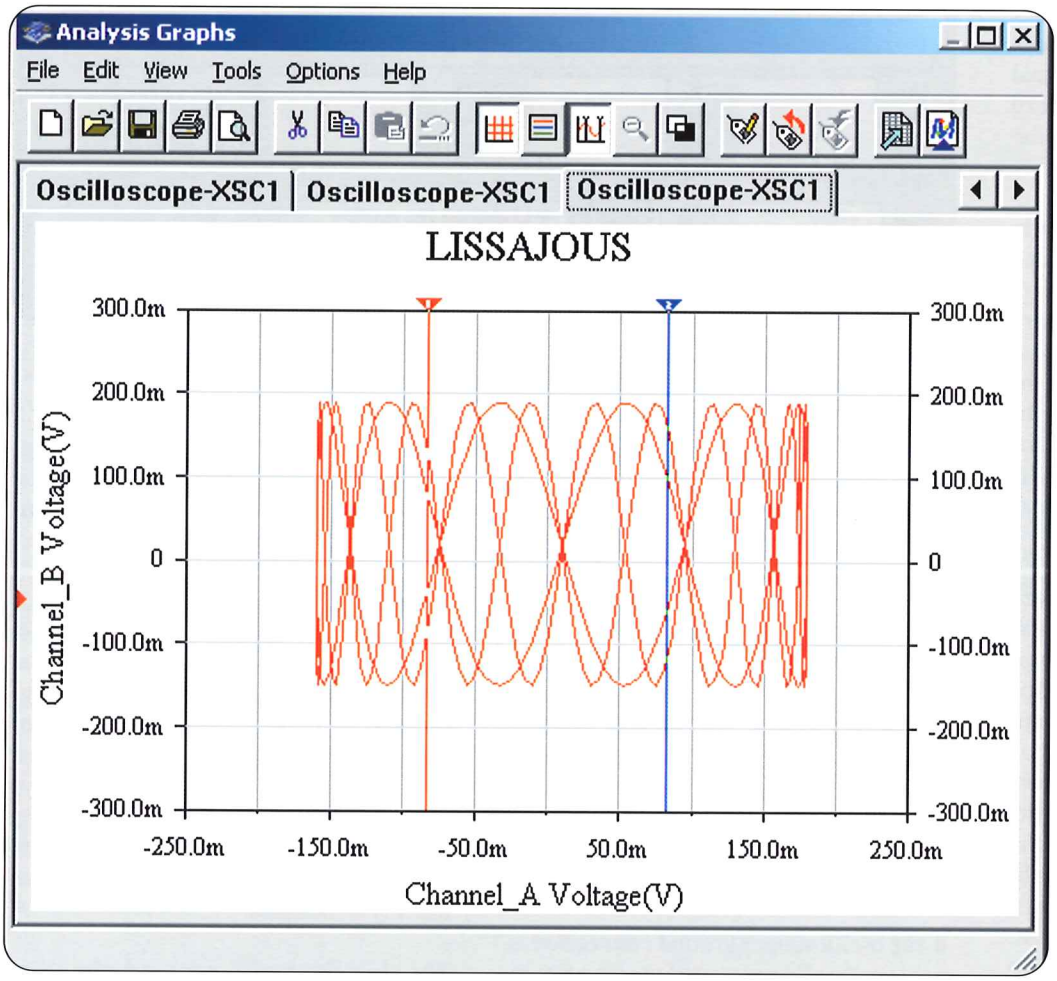


Figure 3 - Using the grapher to make a customized printout of oscilloscope data.

Understanding the SPICE Simulation Engine

An explanation of what goes on behind the scene.

By Herbert Bernstein

Multisim is based on, and fully compatible with the most common international SPICE standard – SPICE 3F5, developed at the University of Berkeley. Georgia Institute of Technology made further enhancements to SPICE 3F5 to eventually produce the latest extension to BSPICE, called XSPICE. Multisim is also fully compatible with XSPICE and employs all of its features. Many semiconductor manufacturers are making simulation models for their products available for download free-of-charge from the Internet. Importing SPICE models is simplified using a component creation Wizard that walks you through all essential steps. You can add vendor SPICE models without having to understand any SPICE syntax at all.

The simulator uses mathematical descriptions to calculate numerical solutions for your circuits. These calculations require all components in the circuit to be represented and described using mathematical models. The more accurate the component models, the more the simulation results will correspond to real life values. Each circuit is described using a series of simultaneous non-linear differential equations. The primary function of the simulator is to find numerical solutions to these equations. A SPICE-based simulator converts these non-linear differential equations into a series of non-linear algebraic equations. These equations are further linearized using the Newton-Raphson method. The resulting set of linear algebraic equations, a sparse matrix equation system, can be solved effectively using the LU factorization method. The simulator works using the following four phases:

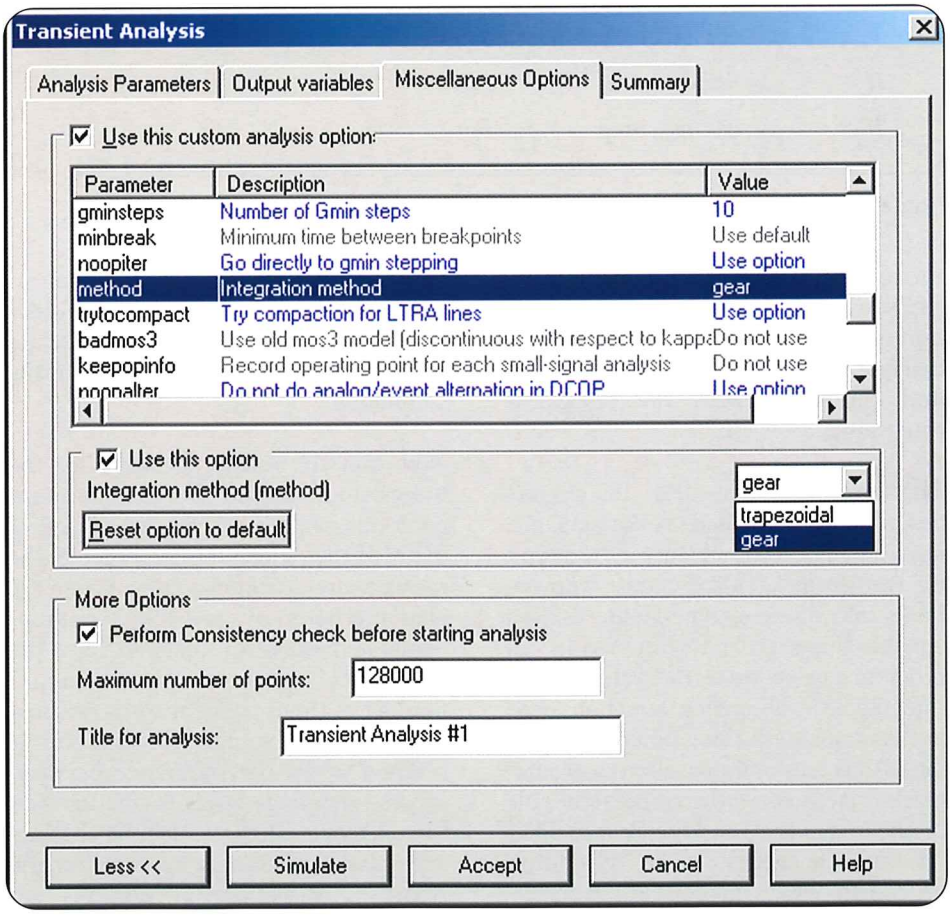


Figure 1 - Multisim lets you control how the simulation engine operates, including the type of integration method used.

INPUT

Once you have created a circuit schematic, assigned values to the respective components, and selected an analysis type, the simulator reads in the circuit data once the simulation starts.

CONFIGURATION

The simulator designs and checks a set of data structures that contain the complete description of the circuit. Every error is detected immediately and displayed so that the input can be corrected.

ANALYSIS

The analysis type you selected is performed. This phase demands the most CPU time and is the core phase of the circuit simulation. In the analysis phase, the circuit equations are created, calculated, and solved in accordance with the selected analysis. All data is output directly and/or made available for further processing.

OUTPUT

In this phase, the results are displayed via the virtual instruments. Alternatively, if analyses were run, results are output to the grapher. In the circuit, all common points created by wires and/or connecting points are designated as nodes. The simulator operates by calculating voltages on all nodes. In the case of a branch in the circuit that links two nodes, separate currents are assigned to each node. The equation system is created using a general circuit analysis method called MNA (Modified Nodal Approach). The modified nodal admittance matrix is "weak" since it has more zero than non-zero entries. The circuit equations can be solved with a concatenated list by using non-zero expressions.

This method is known as the sparse matrix technique and generally requires less memory. The simulation is also performed much faster in this way. The simulator solves equations for linear and non-linear circuits using a unified algorithm. The solving of a linear DC equation is treated as a special non-linear DC circuit. The modified sparse node matrix equation system (a set of simultaneous, linear equations) is calculated on the basis of LU factorization. This includes the factoring of Matrix A into two triangular matrices (a lower triangular matrix L and an upper triangular matrix U) and the solving of both equations by means of forward and backward substitution. A number of effective algorithms are used to avoid numerical problems with the modified node formation, to increase numerical calculation accuracy, and to maximize solution efficiency. These include:

- A classification algorithm that improves the matrix requirements
- A reclassification algorithm that minimizes non-zero expressions for solving equations

A non-linear circuit is resolved by transforming the circuit for each iteration into a linearized, equivalent circuit and then resolving it iteratively using the method described above. Non-linear circuits are transformed into linear circuits by linearizing all non-linear components using the Newton-Raphson method. A general, non-linear circuit is transformed into a discrete, equivalent, non-linear circuit and calculated with the respective time values.

When the trapezoidal method is applied, the following approximation is used to discretize the differential equations:

$$V_{n+1} = V_n + \frac{h}{2}\left(\frac{dV_{n+1}}{dt} + \frac{dV_n}{dt}\right)$$

where

V_{n+1} = present unknown voltage value

V_n = previous time-point solution

h = time step length

n = time interval.

The first-order Gear integration is the popular Backward Euler method. The second-order variable step size Gear integration formula is:

$$\frac{dV_{n+1}}{dt} = \frac{2h_n + h_{n-1}}{h_n(h_n + h_{n-1})} V_{n+1} + \frac{h_n + h_{n-1}}{h_n - h_{n-1}} V_n + \frac{h_n}{h_{n-1}(h_n + h_{n-1})} V_{n-1}$$

where

V_{n+1} = present unknown solution

V_n = previous first time-point solution

V_{n-1} = previous second time-point solution

h_n = present time step

h_{n-1} = previous time step

Figure 2 - Description of the trapezoidal and gear integration formulas.

The method for non-linear DC circuits described above is used. A dynamic circuit can be transformed into a DC circuit by transforming all dynamic components into discrete components using a suitable numerical integration rule. In order to approximate the value of the integral of the differential equations used in the time range calculations, this simulation has two optional numerical integration methods — the trapezoidal rule method (standard) and the Gear method (1st to 6th order). The maximum order up to which integration can be performed can be set in Multisim using the Simulate > Analyses > Transient Analysis > Miscellaneous Options. A higher order theoretically produces more accurate results, but will however slow down the simulation.

Note that the maximum order for the integration method is the maximum order that can be used. However, the simulator always selects the best order for the relevant circuit automatically. Given the characteristics of non-linear components, it may be necessary to solve the admittance matrix for each timestep a number of times before it converges to a solution. The solution for a point is reached when the difference between successive voltage levels is smaller than the tolerance calculated for the absolute and relative tolerances specified in the Analyses Miscellaneous Options tab described above.

Using Simulation for Better Designs

Once a complex rarity, board-level analysis is now considered a necessity. Some tricks of the trade, and why you shouldn't send your design out without simulation.

By Campbell Britton

Mainstream PCB designers often avoid circuit simulation because it can seem unduly complex and intimidating. This is not surprising, considering that simulation has historically required specialized knowledge of simulation and device modeling. But today these outdated perceptions of simulation are disappearing. Savvy designers are discovering that the minimal time investment in simulating a design can result in fewer iterations and less chance of nasty prototype surprises. Engineers who simulate their circuits at the front end of the design process can significantly reduce the number of design cycles. Here is a brief update on the evolution of simulation software and some tips for maximizing the process.

A few years ago engineers and designers treated simulation like the plague because of the burdensome syntax that had to be understood. Today's designers find that effective design verification is feasible because simulation tools have become very easy-to-use, providing accurate results quickly in an environment that is flexible enough to fit the front-to-back design flow of most design teams.

Many of the current crop of simulation software tools permit a design generated with the schematic capture tool to be simulated quickly, because each schematic symbol is equipped with a built-in simulation model. This is a vast improvement over the not-so-distant past, when most engineers performing simulation had to completely redraw their schematic in the "capture environment" of their simulation software.

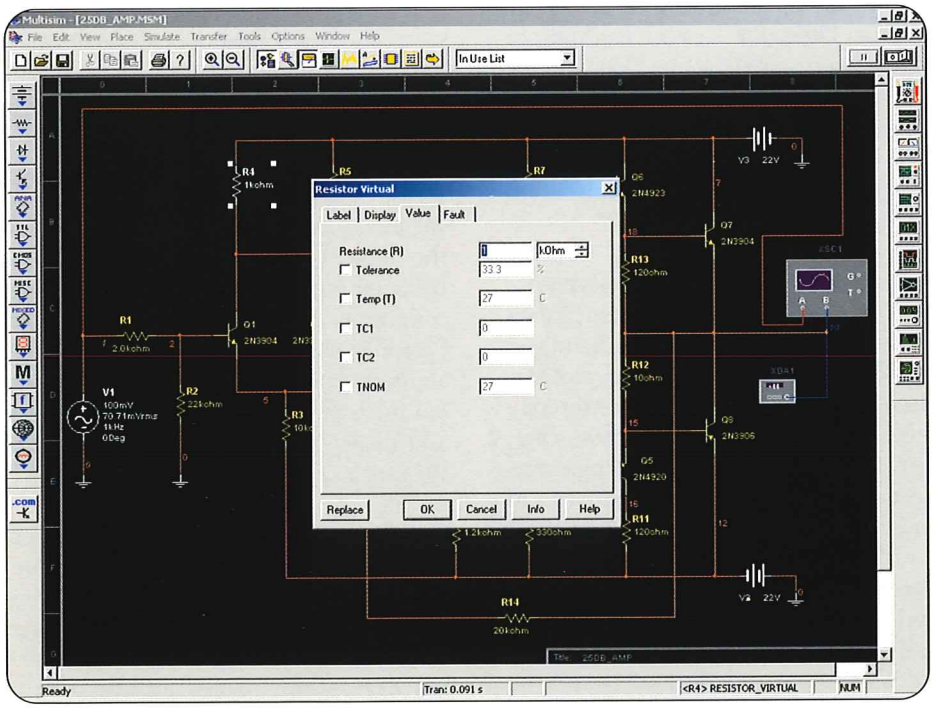


Figure 1 - Circuit with virtual part dialog.

Engineers no longer need to be experts in simulation technology to analyze the performance of a circuit, and they don't need to learn complicated SPICE or HDL syntax. With today's simulators, designers can easily create various proof-of-principle scenarios well before the prototype is built.

FIVE SIMULATION TIPS

The following five tips will lead to successful simulation and more accurate board designs.

1. Simulate using ideal models and add complexity incrementally.

Often, a design is based on standard configurations in which each part of a circuit is described and then refined over a number if iterative cycles. At this stage, it is best to begin simulation using ideal models, or at least simplified models of the components. The simulation will generally converge more quickly because the model does not have all the parametric data associated with its real-world component. (Convergence is the mathematical ability of the simulation engine to solve the equations it uses to represent the circuit). Early in the design cycle, ideal models will offer faster simulation speeds and provide sufficient accuracy to determine if the design is headed in the right direction.

Newer simulators usually offer some type of "virtual" components that allow the user to select any theoretical value and replace it later with a part from a library of actual components. Interactive parts permit parameters of a component to be varied during simulation, and permit observation of the effects on the circuit's performance in real time. At the outset, it is usually appropriate to ignore the para-

sitic effects that add complexity to the models and lengthen the simulation time. Once the general circuit operation has been obtained, component models can be replaced with those that more precisely represent the actual component.

2. Simulate critical areas of the design.
A structured modular approach permits isolation of each element in the design and ensures each circuit block is behaving as expected before being integrated into the whole. For all but the most straightforward designs, the best method for achieving this is a hierarchical approach. This approach leads to the creation of reusable modules that can be used in other designs at a later time.

Most of those who perform design entry with schematic capture software do so as part of their standard design flow. Employing this "block design" method simplifies the use of simulation software, since each sub-block can be simulated using the expected stimulus at the interface points. Time was, simulation users complained about the difficulty in generating the necessary stimuli, but today's software eases this task by providing a number of techniques for creating the required inputs to each block.

The stimulus can be generated internally by the simulator using a wide variety of sources, including standard waveforms, various modulators, controlled sources and complex polynomial functions. Look for EDA tools that offer virtual instruments such as function generators and word generators to drive the circuits. (Virtual instruments operate much like their real-world counterparts). Also, the output signal of an earlier stage can be used as the input signal of the next. Externally generated stimuli can be stored to a file for later importation into the simulation in a piecemeal manner.

Examples of dividing a circuit into blocks for simulation include the following: an amplifier stage in which the signal-to-noise ratio must be thoroughly understood; the impedance matching of different stages in a network; a test bench that accurately represents real-world conditions. An additional example might be a mixed analog input stage to an analog-to-digital converter (ADC) is in one block and the digital stage is in a separate block.

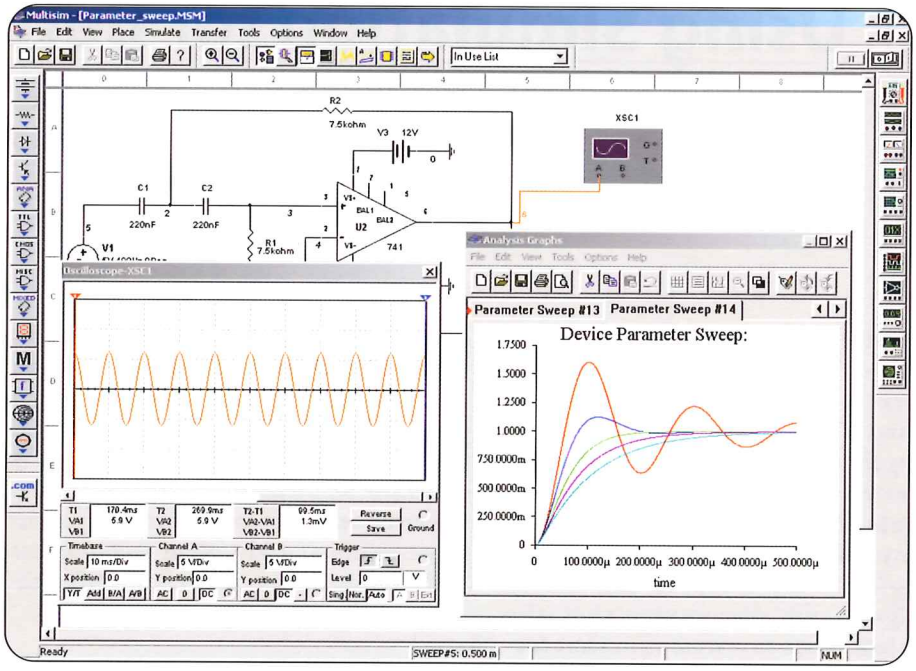


Figure 2 - Screen shot illustrating analysis results. Start with the virtual instruments (oscilloscopes, bode plotters, spectrum analyzers) and work up to waveform analysis.

3. Analyze the results, starting with less complex methods first.
Simulation software is ultimately used to examine the signals at various points in a circuit. There are several methods of increasing sophistication that can be used to analyze the signals in a circuit. Consider these three different alternatives in ascending levels of complexity: virtual instrumentation, simulation analyses and post-processing.

Measurement of a circuit's performance and functionality can be accomplished by connecting virtual instruments — including oscilloscopes, bode plotters, spectrum analyzers and others directly into the schematic design. Most engineers have operated scopes and logic analyzers, so using virtual counterparts in simulation software should be intuitive.

Circuit performance can also be measured and evaluated with a vast array of analyses. These analyses use mathematical calculations to help understand the operation of the circuit in ways not possible in the real world. To obtain the baseline performance of the system using a SPICE simulator, begin the analysis in the time domain or frequency domain. Transient analysis computes the circuit's response with respect to time. AC analysis is used to determine circuit response in the frequency domain. The DC operating points are determined automatically by the simulator, though it is possible to set initial conditions for specific circumstances.

As the design progresses, various statistical analyses can be used to provide a thorough understanding of the circuit behavior under a variety of operating conditions. Note that statistical analyses typically perform either transient or AC analysis, but they vary model or circuit parameters over a specified range and display results at each step within the range.

Some of the most important analyses include Monte Carlo, Worst Case and Temperature Sweep. Monte Carlo analysis computes circuit response to changes in component values by randomly varying device parameters according to a

user-configurable distribution. For example, bias resistances can be varied according to a Gaussian distribution to measure the effect of component tolerances on the design. Worst Case analysis permits the effects on circuit performance of variations in component parameters to be explored. Temperature Sweep analysis varies the temperature over a definable range and displays the voltage or current levels at specific circuit nodes for each temperature value. Other useful analyses include Pole-Zero analysis, which can be used to gauge the stability of circuits, and Fourier analysis, which takes a Fourier transform of the transient analysis to obtain voltage component magnitudes versus frequency.

Post-processing of signals that are normally waveforms, not single data points, is commonplace in simulators today. The post-processor permits manipulation of the output from analyses performed on a circuit, plotting the results on a graph or chart. Waveforms can be added, subtracted, multiplied, and so on. This capability is very important to fully understanding a circuit, and it is difficult or impossible to do so without post-processing. Types of mathematical operations that can be performed on analysis results are not limited to simple arithmetic functions, and can include trigonometric, exponential, logarithmic, complex, vector, logic and more.

4. Consider HDL models for complex digital ICs.

Digital devices can be modeled in several ways. For smaller ICs, the best method for modeling is using SPICE and the digital extensions built into the simulator. Your EDA vendor can confirm that its libraries contain simulation models for all of its parts, and that those models are not constrained to one simulation language, such as SPICE.

For example, think of the 7400 series TTL chips or 4000 series CMOS devices. Most of these devices typically use smaller scale integration and fewer gates, and are adequately modeled using SPICE. However, larger ICs with many thousands of gates are best modeled with VHDL (using standard IEEE 1076-93) or Verilog (using standard IEEE 1364). Writing a SPICE model for complex devices is not practical in most cases. Such complex digital chips can even include programmable devices. FPGAs and CPLDs can be programmed in either VHDL or Verilog and then integrated into the overall design using their HDL code as the simulation modeling language.

Co-simulation, as this method is known, integrates the simulation results from the HDL simulators and the SPICE simulation engine and generates a combined set of results that can be analyzed by the engineer. With co-simulation, all devices on a board can be simulated as one complete circuit. The need to create elaborate testbenches is reduced because the input stimuli to the device under test can be the result of the SPICE or HDL simulation. This is an important and relatively new technique, as older simulators could only support one simulation language. Again, check with your EDA vendor to find out if their simulation software offers a co-simulation capability.

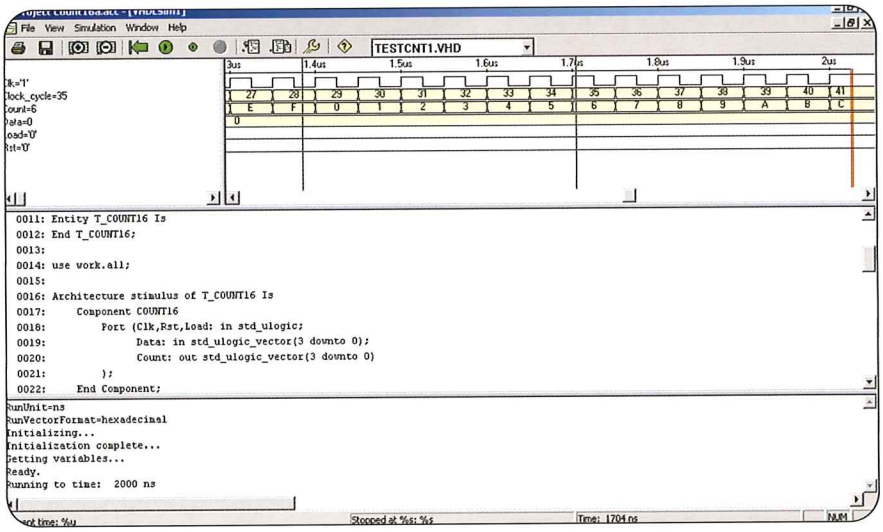


Figure 3 - Screen shot of Multisim VHDL.

5. Models, models, models.

To enable easy simulation with your schematic software, remember the distinction between symbols and models. For EDA software to handle simulation as a straightforward step after capture, it must contain symbols as well as models. Remember that models are to simulation as symbols are to schematics. While modeling a component can be technically complex, the best EDA software includes extensive libraries of models to take this complexity off the end-user's plate. Again, check with your EDA vendor to confirm that its libraries contain simulation models for all of its parts, and that those models are not constrained to one simulation language.

In addition, to accommodate new devices entering the market, a mechanism must be in place to add new models to existing libraries. This can be handled in two different ways. First, simulation software should include model makers that permit databook parameters to be entered directly. The databook parameters are then converted into SPICE parameters for use by the simulator. (Note that databook parameters are not the same as SPICE parameters, although in some cases the parameter names may be similar).

The second method for obtaining parts is by way of the Internet. Most manufacturers that offer SPICE or HDL provide component models through their Web sites.

Simulation is one of the best ways to complete the design faster and with a high degree of confidence. Because today's simulation software is easy-to-use and available from most EDA vendors, there is no reason to avoid adding this high-value step to your design flow.

Nikhef and CERN Choose Ultiboard

Leading scientists transfer particle detection technology to traditional industry.

By Dan Harris & Andre Veenstra

CERN has a long tradition of developing exceptional technology for research and then transferring these breakthroughs to industry. The World Wide Web, for example, was developed at CERN to improve communications among its members. Currently, Nikhef and CERN are working on bringing advanced particle detection technology to more every day applications.

CERN is the world's largest particle physics center and one of the world's largest scientific laboratories. For half a century CERN and its scientists have been investigating the mysteries of the world trying to discover what matter is made of and what binds it together. Their investigation proceeds by accelerating particles at extremely high speeds and then colliding them together. By observing the behavior of particles during these collisions, scientists can deduce the nature of matter.

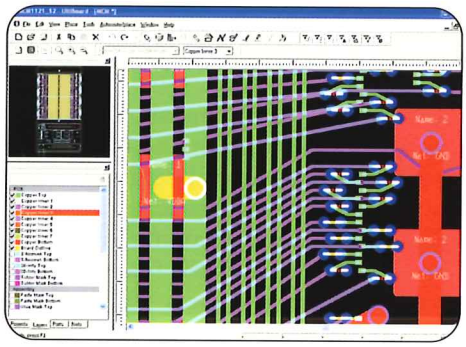


Figure 1 - Nikhef High Density Interconnect board in Ultiboard.

Nikhef (National Institute for High Energy Physics in the Netherlands) helps produce the detectors that observe these particles (too small to be seen by the human eye) during collisions. Nikhef and CERN are taking the world's finest particle detection technology used for high energy physics and extending it for use in traditional medical, space, and x-ray imaging applications. While this technology has been used for detecting tiny particles, Nikhef's challenge was to create a board that could sample images of much larger objects. Nikhef's board, unlike traditional CCD imaging boards, operates by detecting individual photons and creates images with no noise. Additionally, images are more sensitive and can be taken with 30 times lower radiation exposure when used in x-ray applications.

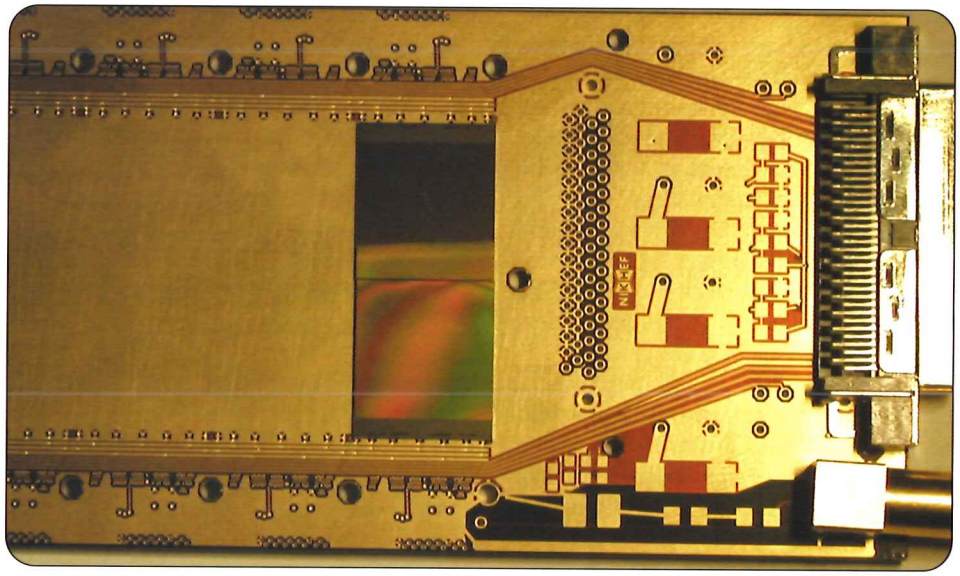


Figure 2 - Completed High Density Interconnect Board.

Nikhef needed to create a High Density Interconnect board to support the particle detection chips, each containing 64,000 pixels. These dense chips required Nikhef to use "Chip On Board Technology" and wire bond the chips to the board in the same way they are normally bonded to their casing. Nikhef used a total of 160 wire bonds using gold plating on the top layer of the PCB.

Nikhef chose to use Ultiboard for this project because they liked that the product was PC-based and found Ultiboard very easy-to-use. The company also uses much more expensive tools but would have needed to buy an extension to those programs to handle the fine-line microvia technology required for their board. According to Nikhef's Jan Visschers, "This high density interconnect technology board hit all the normal resolution boundaries with 2 tau lines, smaller vias, and extreme magnification needs. Ultiboard can do everything we want". Ton Boerkamp of Nikhef added, "We got very good support from the technical team at Electronics Workbench. They found solutions or workarounds for all our problems".

Nikhef completed the board comfortably and within the predicted development time. The design passed through prototyping without any problems and at the time of writing the board is under production. Nikhef together with CERN are now working on modifying the board to be able to accommodate increasingly large images.

Board Properties:

- 9 layers: 4 epoxy and 5 kapton build-up
- 1840 microvias
- 366 through-hole vias
- 60 um tracks
- 56 mm x 110 mm board size
- 15 um copper
- Staggered microvias

Simulation and Analysis of High-Frequency Circuits

By Alexander Ehle

The simulation and analysis of higher-frequency circuits is not without its problems. Couple this with the co-simulation of different technologies, and the limits of most simulation systems are quickly reached. Multisim supports the simulation and analysis of RF models. Both high-frequency and low-frequency circuits can be co-simulated with digital circuits and programmable logic devices (FPGA/CPLD).

For analysis in the high-frequency range, there are special virtual instruments whose functionality and handling are based on those of real laboratory instruments. Multisim's Network Analyzer uses the functionality of the HP8751A and HP8753E from Hewlett-Packard® and is quick and easy-to-use. The simulation results can be viewed in Cartesian or polar form and as a Smith Chart. You can edit the display or scaling with just a click of the mouse. You can also view S, H, Y and Z parameters as well as the stability factor of a network.

The Network Analyzer is easily connected to input and output points in the circuit and then the simulation is started. Shortly afterwards you see all of the simulation results, which you can analyze and evaluate using a sophisticated range of functions. Thanks to an export function, all data can be transferred to other applications including spreadsheet programs and mathematics programs.

The Network Analyzer has a range of additional functions such as impedance matching (Network Matching) and a RF Circuit Characterizer. Impedance matching allows quadrupoles with different input and output configurations (equivalent circuits consisting of concentric elements) to be examined. A wide range of information and setting options provide the designer with valuable information about a planned design.

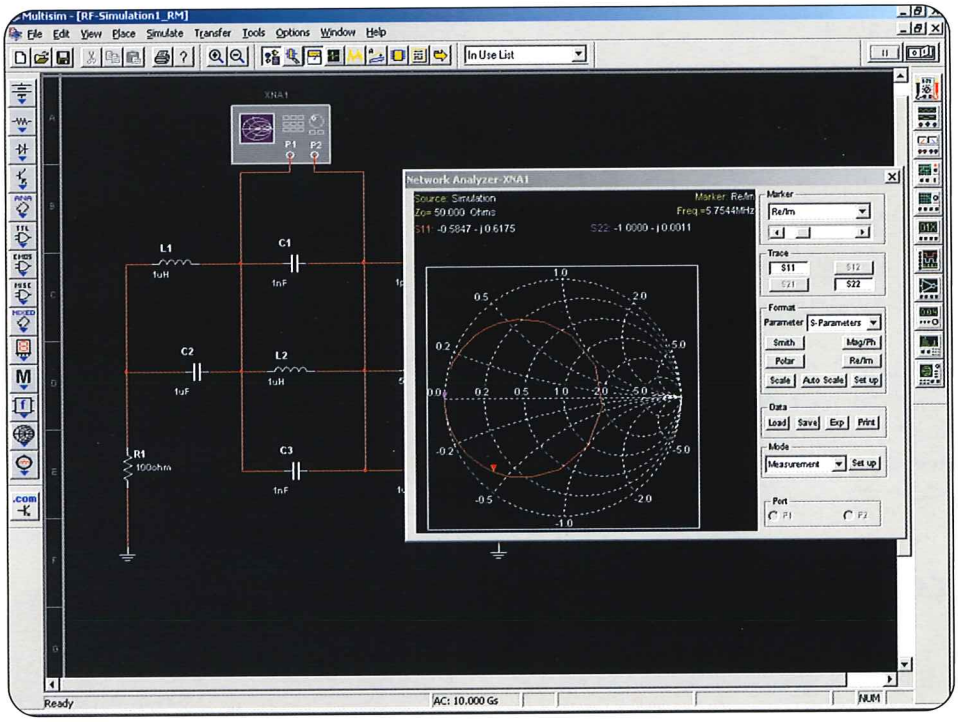


Figure 1 - The Multisim Network Analyzer.

With a bandwidth of up to 4 GHz, the Spectrum Analyzer from Multisim covers the entire frequency range from low to high frequency. Once again, operation is based on that of real instruments, resulting in intuitive handling.

Span control is individually configurable. The scaling can be set to dB, dBm or linear with just a click of a button.

For the purposes of analyzing the simulation results, a reference line can be shown in the Spectrum Analyzer display and the diagram can be analyzed with the aid of a cursor. The scanning rate of the Analyzer is determined automatically, but can be adapted manually if necessary to optimize conditions for the DFT method.

Apart from the standard SPICE analysis methods, there is also a method for determining the noise figure (NF) in dB. In no time at all, Multisim can calculate the noise figure for any point in a circuit.

Conventional noise analysis is also supported in Multisim and allows the calculation of input or output noise in sources, semiconductors and passive components.

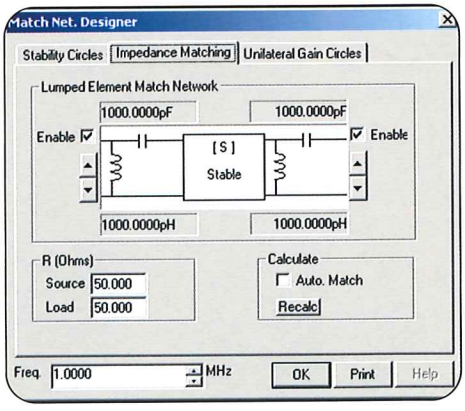


Figure 2 - Network Analyzer impedance matching.

The RF Design Module also includes an RF library. This library contains RF MOSFETs, etc. as well as various passive components and line models. Individual models can be created with the aid of special model generators. Models can be created for the following RF components:

- Spiral inductor
- Inter-digital capacitor
- Waveguide
- Microstrip conductor
- Open microstrip conductor
- Stripline
- Stripline bend
- Lossy line model

The models are defined in self-explanatory windows that are structured in the form of a datasheet. The default values use geometric data and material constants, for example.

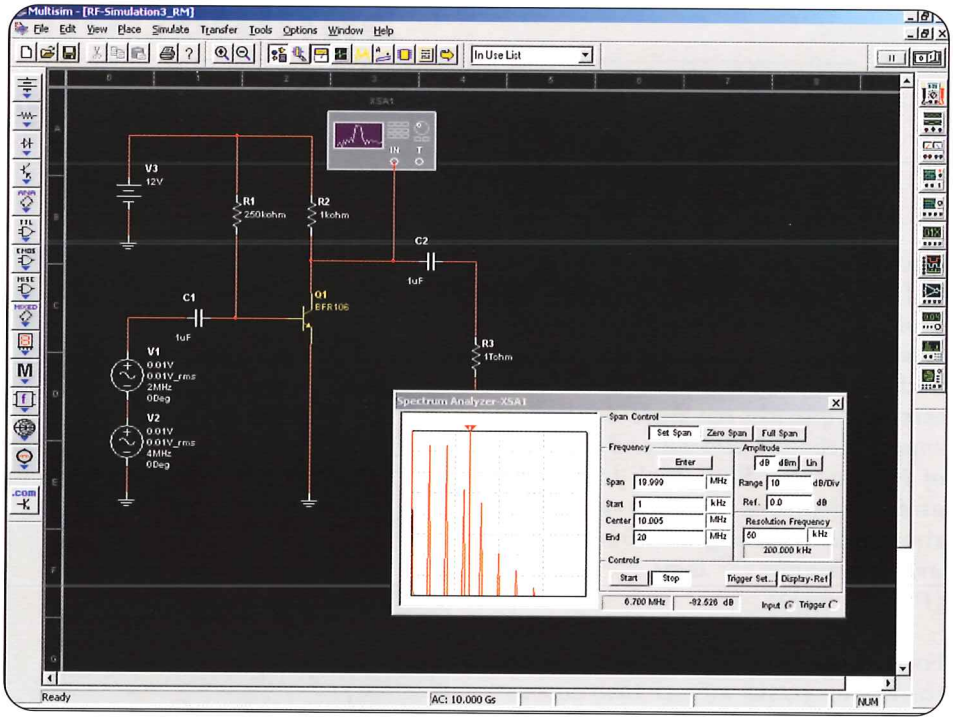


Figure 3 - The Multisim Spectrum Analyzer.

CONCLUSION

Compared with dedicated HF simulators, Multisim offers a broader range of applications combined with ease-of-use. The menus and dialogs make the system both easy-to-use and effective for new users as well as experienced designers. Unique design and analysis methods usually found only in high-end and high-price products, make Multisim a valuable and indispensible resource for everyday circuit and system design tasks.

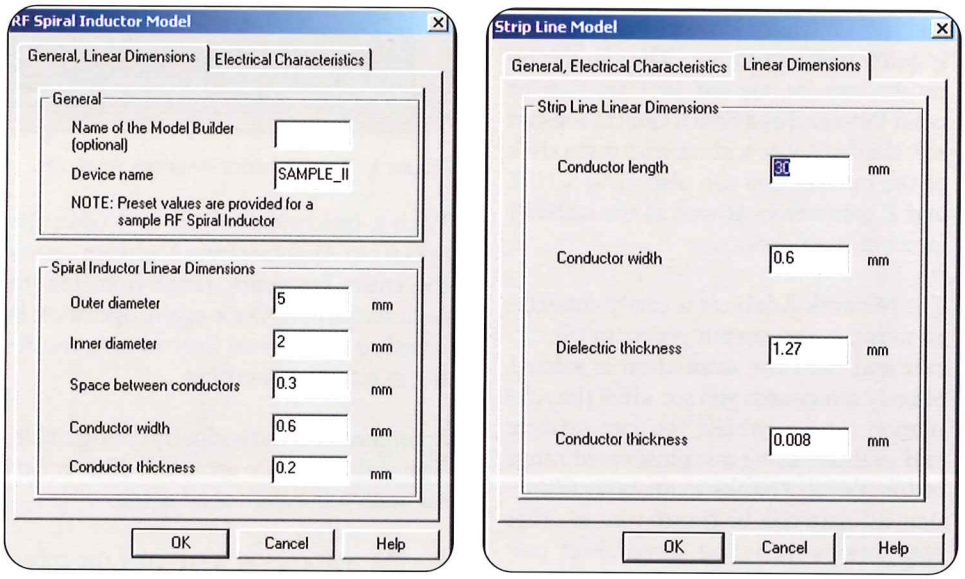


Figure 4 - Model generators for RF components.

Getting More from Ultiroute

By Campbell Britton

Ultiroute, from Electronics Workbench, is a next-generation autoplacement and autorouting tool that seamlessly integrates with the powerful PCB layout package – Ultiboard. With so many overly complex routers on the market, Ultiroute is a refreshing alternative. All the placement and routing intelligence is built in, and can easily be configured through the program interface. Complex scripts are not required to route fully manufacturable boards. With the tips below in mind, you will be routing boards faster, more efficiently, and in most cases at less cost than with any other product.

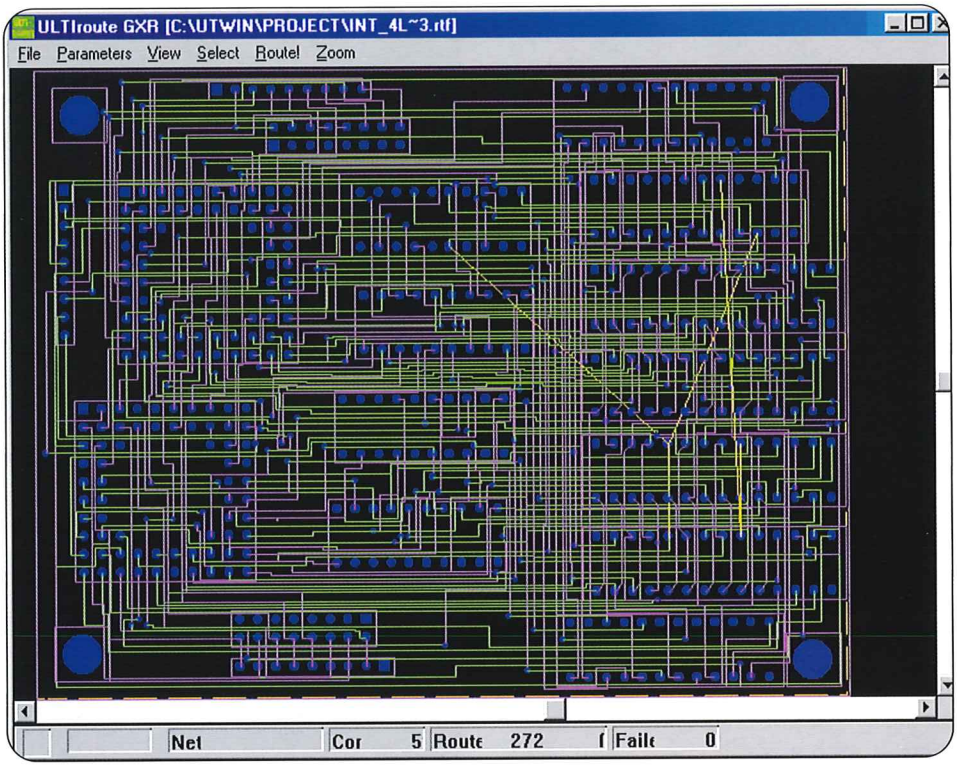


Figure 1 - Ultiroute making final connections.

PLACEMENT TIPS

Autoplacement

To minimize trace lengths you should follow a simple process of using Ultiroute's autoplacement functionality, with automatic part rotation, in conjunction with the more traditional manual placement. This will deliver a board that can be routed faster and more efficiently as the internal algorithms of Ultiroute determine placement based not only on the physical footprint, or special constraints of the component, but through the minimum trace length as well.

CONFIGURATION AND SETUP

Cost Factors

You can adjust the powerful cost factor settings to control how Ultiroute weighs its various routing strategies. Small adjustments, either slight increases or decreases in these values will provide better results. Be careful not to alter too many factors at one time as this can have a detrimental effect on the overall routing results.

Trace Bias Direction

By simply determining the preferred trace bias direction at the outset you will obtain faster and tighter routing results. Select either horizontal, vertical or both on a per layer basis.

ROUTING

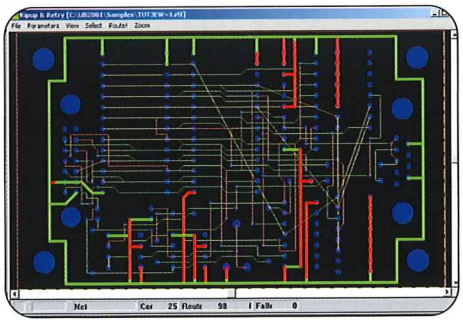


Figure 2 - Ripping up and retrying for better connections.

Initial Autorouting

Never set up your initial routing parameters to be so complex and rigid that the board becomes unrouteable. Traces are placed based on their complexity factor, which at the outset is the longest to shortest length of the Manhattan route. This will route the majority of traces the first time. Then in further iterative passes, with tighter constraints, you will achieve your fully routed board.

Rip-up and Retry Parameters

Ultiroute gives you comprehensive control over the parameters that determine the overall 'effort' for Rip-up and Retry routing. The Rip-up trees, Rip-up depth and Rip-up retries will limit the number of traces to be ripped up, its persistence in finding a suitable path and the number of retries before it moves on. Small increments here, coupled with autorouting passes will quickly get the board fully routed.

Combination of Grid-Based and Grid-less Routing

The success of Ultiroute is due in part to its unique application of a combined grid based, and grid-less routing algorithm. The main routing engine routes on a grid where necessary, but automatically switches to grid-less when necessary. This gives the user the great benefit of fast routing times on grid, and routing of more difficult traces off grid. Make sure Ultiboard is configured correctly, through the routing options dialog, to gain maximum benefit from this ground breaking technology.

Via Grids

Vias are needed in just about every board design today, so Ultiroute will automatically place them for you, when necessary. You should set the via grid to your specific technology and design constraints, be that on grid (50 mil or 100 mil) or off grid. On grid of course, will greatly assist in manufacture, whereas off grid will utilize unused space in tighter designs.

Security Copy

All professional engineers know that modern board design is an iterative process, with a tweak here and a nudge there. However sometimes after constant tweaking a completed design may not be to the liking of an engineer, and he wishes to return to a previous iteration — but where is it? The security copy feature in Ultiroute will automatically save out a backup of intermediate results, providing a simple backward step in the design process that can be highly useful.

OPTIMIZATION

Optimizer and Clean Up Routines

Once a board is completely routed the optimizer and cleanup routines in Ultiroute will search through the design, identify and rectify 'problem' traces that are having an overall detrimental effect to the routing results. Any remaining open connections will also be routed. You can set the number of passes, up to a maximum of 99, far in excess of what will usually be required.

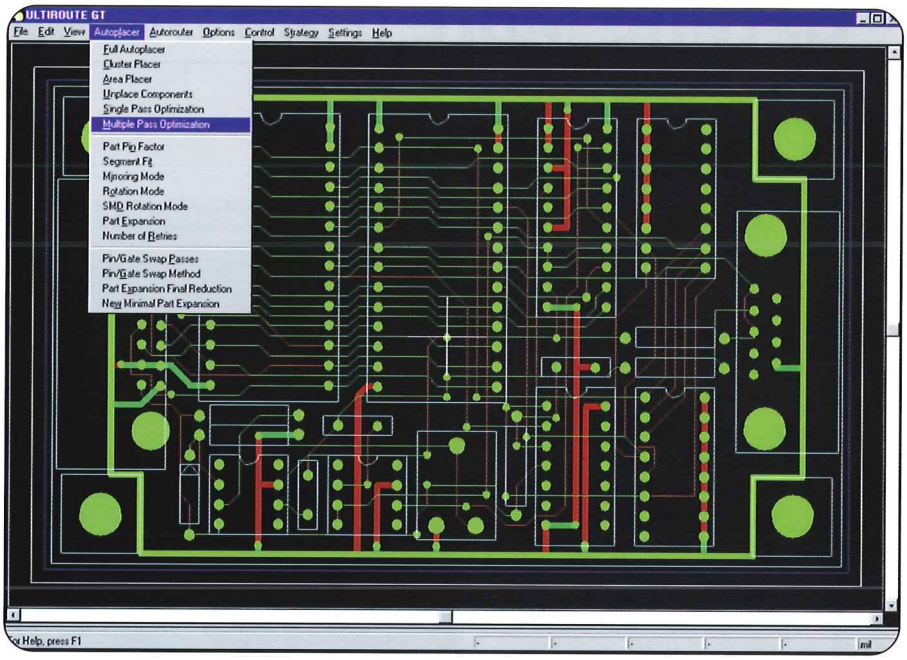


Figure 3 - Choosing optimization settings to improve trace layout.

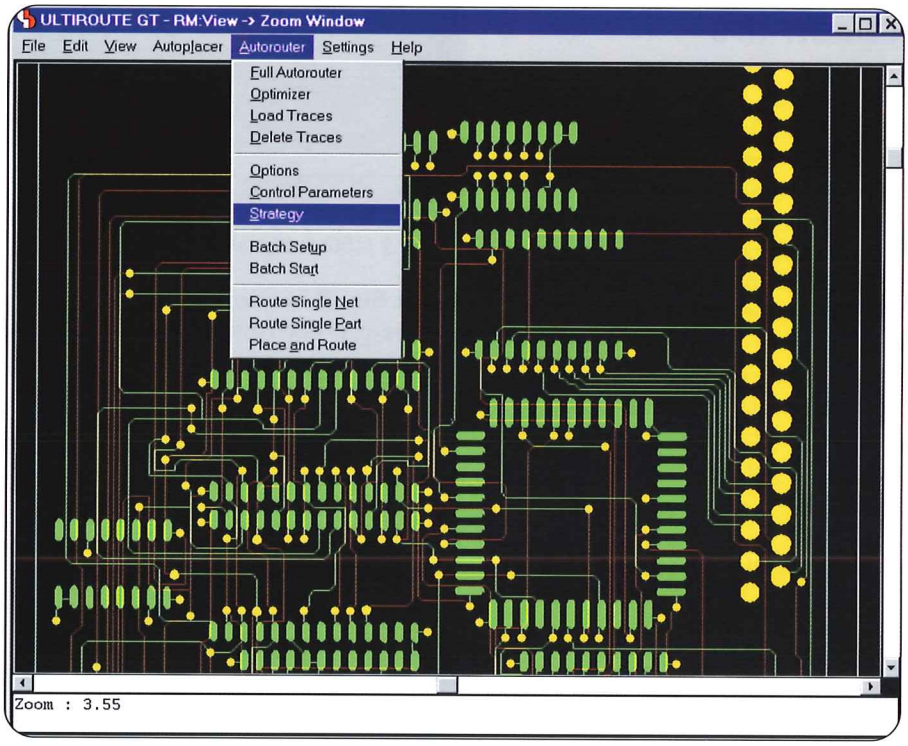


Figure 4 - Choosing autorouter strategy settings.

Via Optimization

The optimizer eliminates unnecessary vias and smooths wire bends to reduce manufacturing costs. Cost factors can be set to minimize via counts or trace lengths as needed.

Re-thinking the User Interface

How an efficient design environment speeds up repetitive PCB layout tasks.

By Dan Harris

PCB layout engineers can spend weeks or even months laying out a single board. Because of this time intensive work, user interface is one of the most critical elements of PCB layout software. An efficient design environment is one of the most significant elements which leads to efficient and productive design.

Creating PCBs is an extremely repetitive task. A single board may require the placement of hundreds of parts and thousands of traces. When performing functions this many times, users will want to customize the program's interface to suite their preferences. Ultiboard contains a completely customizable user interface. In addition to being able to rearrange and resize elements of the screen, users can also change the contents of toolbars, menus, and shortcut keys. By creating toolbar buttons for frequently used functions, users can reduce the amount of mouse clicks needed to navigate through menus. Similarly, by assigning keyboard shortcuts to commonly used actions, users eliminate the need to move their mouse away from the work area and up top to menus and toolbars. While this may not seem like a great savings to most people, good layout engineers know that this can significantly speed up their work and reduce mouse strain. Ultiboard lets users save their individual interface preferences (menu, toolbar, and shortcut key structures) in their own user configuration file. In that way many people can use the same program, each with their own style of user interface.

Because placing parts and placing traces are the most frequently performed functions in PCB design, Ultiboard has a number of features to simplify these tasks. The program displays a list of parts used in the design (see Figure 1). One can simply click-and-drag a part from the list to the design. As the mouse moves from the list to the work area, the selected part will be attached to the pointer. The program also has a sequencer option so that as you place a part, the next part from the list instantly attaches to your mouse pointer. The parts list can be sorted on any part property so that one can, for example, sort the list according to the number of nets each part has to already placed parts on the board. Then, by first placing the parts from the top of the list, one gives priority placement to devices requiring close proximity to those footprints already located on the board.

Ultiboard has a "Follow-me" trace placement tool that autoroutes from a source pin to your mousepoint as you move around the screen. This interactive method of trace placement lets you "guide" the path of the trace using your mouse without having to manually select each bend and turn as you navigate traces around obstacles. And when you get close to a destination pad, the router has a "Magnetic Attraction" that effectively pulls the trace in to complete the connection.

Another time saving device when routing is the "Connection Machine" that effectively autoroutes an entire trace by simply clicking on a ratsnest line. This extremely fast approach to creating connections instantly creates a connection between the two nearest pads on the net and is ideal for completing bus connections.

Another challenge for PCB designers is that they must manipulate objects on a very dense screen: traces, copper poly-

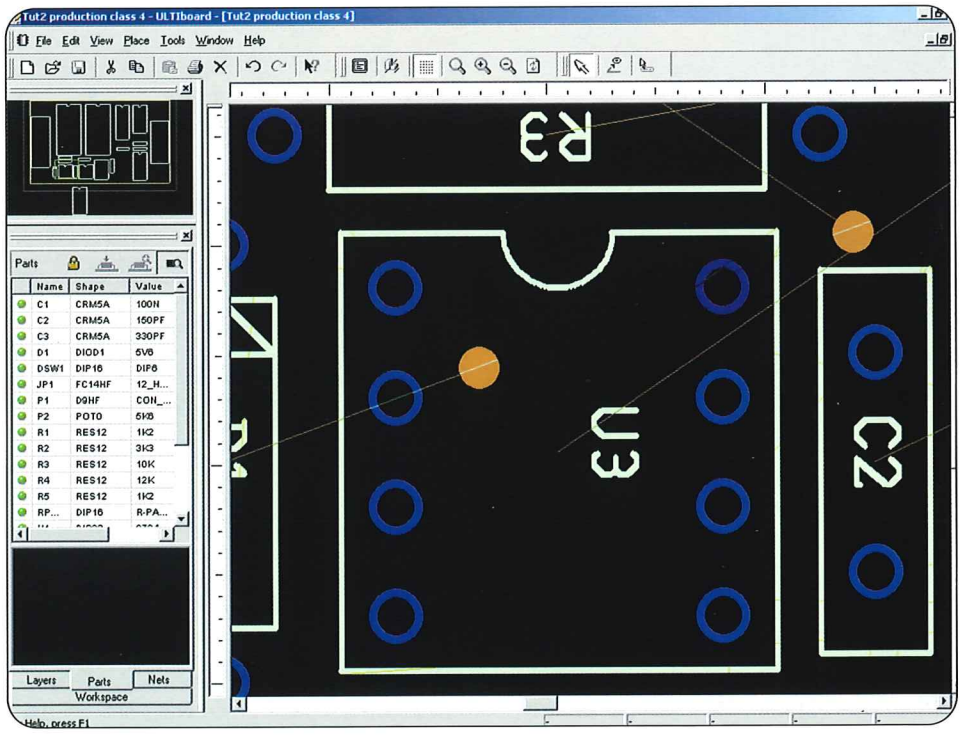


Figure 1 - Multisim's parts bin (left of screen) gives you full control of shapes on the board.

gons, pads, shape outlines and text all fill the screen and often overlap each other in different layers. A good user interface is essential in PCB design to allow engineers to navigate through the maze of objects on the board and to easily select a desired object from a number of overlapping items.

Layer dimming in Ultiboard is an unique feature that enables the user to "dim" certain layers. Rather than making non-active layers invisible, users can dim these layers so that they do not obstruct their view of the active layer, yet can still see that layer's objects (see Figure 2).

Another feature useful when working with multi-layer boards is the treatment of overlapping traces. When copper traces or copper areas overlap each other on the screen, the overlapping segment is displayed in a new color. This is a much better approach than displaying just one copper segment and making the other invisible. By displaying overlapping copper in a different color users can, for example, see all the traces on the bottom layer of a board even if there is a large copper area on the top layer above (see Figure 3).

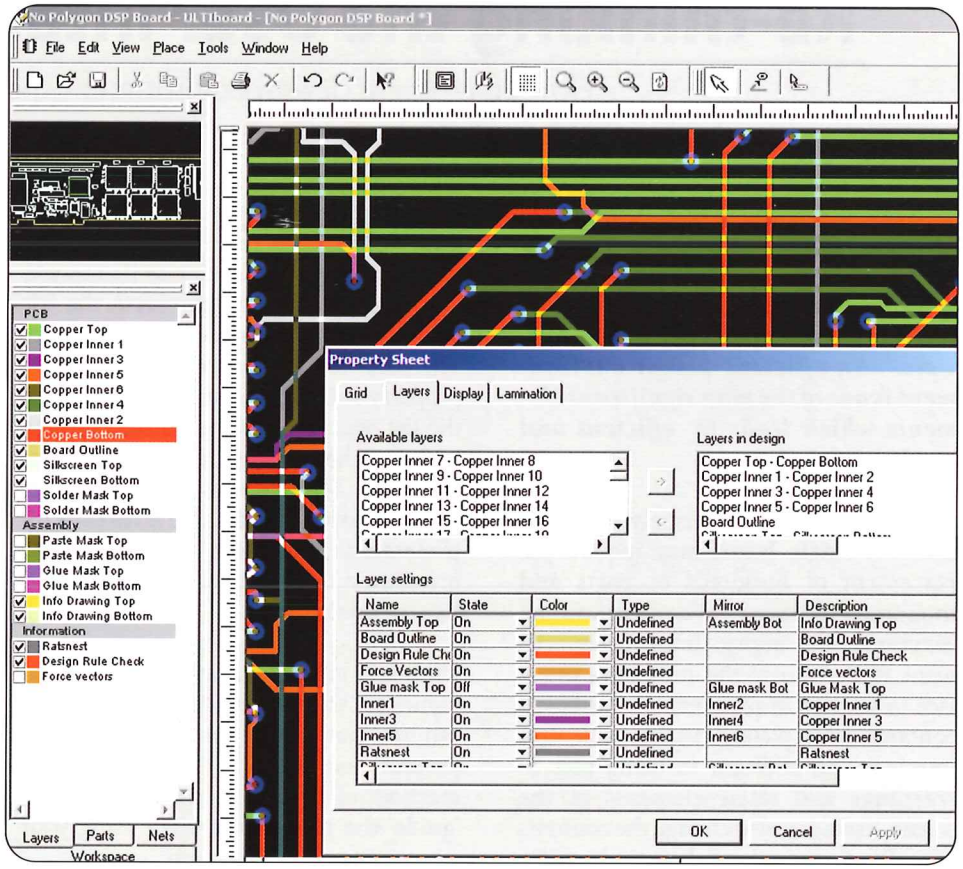


Figure 2 - Viewing different layers.

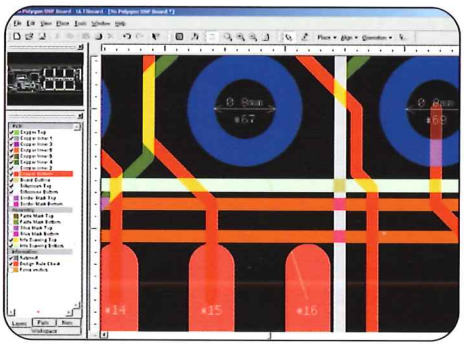


Figure 3 - Viewing traces on different layers.

Selection filters provide an easy way to select a specific item from a number of overlapping objects on the screen. Ultiboard provides selection filters for pads, text, copper areas, traces, and parts. If an user wants to select a trace segment that overlaps a component, they simply turn off the "part" selection filter so that only the "trace" segment will be selected when clicking the mouse on the two objects (see Figure 4).

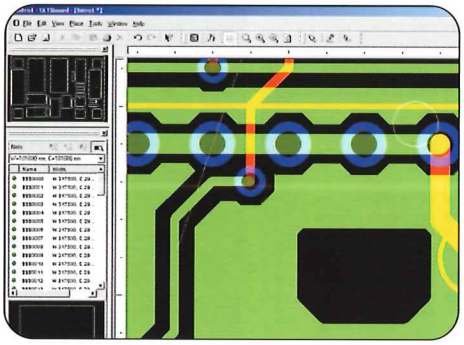


Figure 4 - Filters facilitate selecting objects that overlap each other.

While the Microsoft® Windows® environment provides the world with ease-of-use through menus and toolbars, these useful devices have reduced the effective working area for designers. Ultiboard gives users the option to work in "full screen" mode, which removes everything from the screen except the design itself (see Figure 5). Menu functions can still be used through their keyboard equivalents and through the Right Mouse Button. By maximizing the work area, power users can see a much larger area of the board and work faster by accessing commands with keyboard shortcuts.

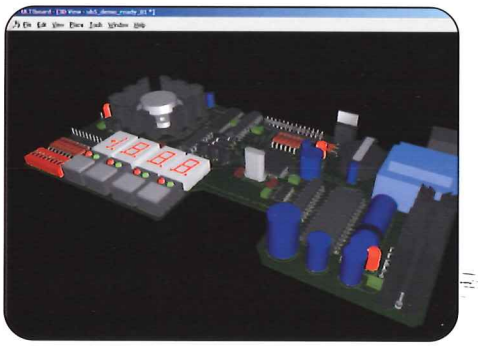


Figure 5 - 3D view in full screen mode.

Efficient and easy-to-use functions can dramatically increase a designer's productivity. Ease-of-use is important so that users can quickly pass a program's initial learning curve. Even a good feature, if difficult to operate, will never get used. Program efficiency is important so that designers can work faster to meet critical deadlines. This is especially true for PCB design where users are constantly under deadlines and even a small inefficiency, when multiplied by the thousands of times it is performed, can be very costly.

dragging a box around them, or by using CTRL+A to select everything. Objects can even be placed in "groups". Any function performed on one member of the group will apply equally and automatically to all other members of the group.

To save time, Ultiboard has an in-place footprint editor that lets users modify footprints directly on the board, without having to use a footprint editor. This feature is also handy when one wants to edit only a single footprint and instantly see the results of the change on the board.

the ratsnest distances are decreasing.

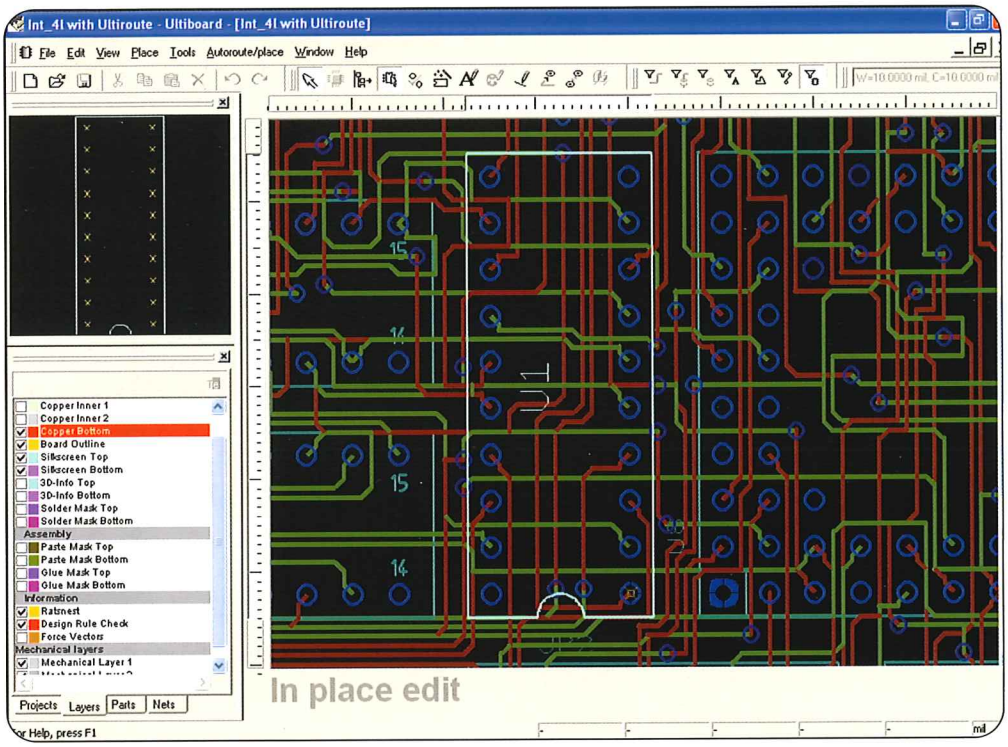


Figure 6 - Making changes to Ultiboard directly on the board using the in-place footprint editor.

Ultiboard offers all the advanced Windows ways of selecting object on the board. Multiple objects can be selected by holding down the SHIFT or CTRL key while selecting with the mouse. In this way, users can perform a function on many objects at a time.

For example, selecting multiple objects and then choosing Edit-Properties lets the user edit all the common properties of the selected objects, all at the same time. Objects can also be selected by

To increase productivity, all functions in Ultiboard operate in real time: ratsnest updates, design rule checks (DRCs), copper area updates, and force vectors. Real time functions give designers instant feedback. For example, with real time DRC, layout engineers are easily able to place parts as close as possible by nudging them together until an error marker appears. With real time ratsnest updating, designers can move a part around the screen and get instant graphical feedback on optimal placement by seeing whether

Tips & Tricks — multiSIM

By Frank Beltzner

PLACING PARTS FASTER

When placing parts in your schematic, there's a good chance that a copy of that same part already exists somewhere in your design. For this reason, Multisim contains an "In Use" list that contains a record of each component or subcircuit placed in the schematic. If you want to place another of the same part, selecting it from the "In Use" list is faster than having to locate the part from libraries.

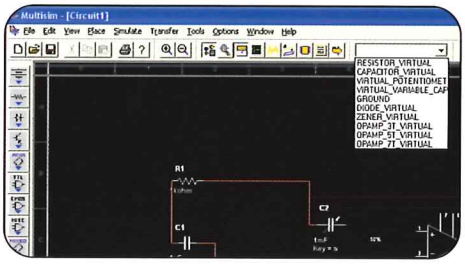


Figure 1 - "In Use" parts list.

Copying (CTRL-C) and pasting (CTRL-V) are of course also useful and quick ways to add more instances of an already placed part. The disadvantage of using copy and paste is that you must find the source part first. Using the In Place list is an easier method to find the already placed component. Using copy and paste is however better when you want to copy a group of parts. You can draw a window around multiple parts to have them all included in the copy function. This technique will also enable you to copy the wire connections as well. Pasting will assign new node numbers for connections, incrementing upward from the highest used node already assigned in the circuit.

SOLVING SIMULATION ERRORS

Encountering SPICE simulation errors does not usually mean that there is something wrong with your circuit, your models, or the engine itself. It more often occurs because the SPICE engine's variable parameters are not suitable for the type of circuit you are running. All Berkeley or XSPICE simulators include a number of miscellaneous settings originally developed at the University of Berkeley. Changing these settings may be needed to resolve problems, including "timestep too small errors". Multisim's default simulation settings are carefully chosen to work best with the majority of circuits. But if you find yourself in a situation where errors occur, here are some things to try under the Simulate> Default Instruments menu:

By default, the "Initial conditions" setting is set to "Automatically determine initial conditions". Many circuits will begin to simulate if you change the "Initial conditions" option to "Set to zero" as all voltages and currents will start at zero.

Newer versions of SPICE use a variable timestep algorithm. This means that larger timesteps are taken when fewer changes in the circuit occur, effectively speeding up simulation time . But when faster changes occur in the circuit, smaller timesteps are taken for higher accuracy. A large TMAX value will speed up simulation during periods of inactivity. The simulator is also constrained to a minimum timestep value that is a set fraction of the TMAX value. And if a smaller timestep is needed than settings permit, a large TMAX value can lead to "Timestep too small error" errors. Try reducing TMAX to 1e-3.

The "RELTOL" setting is used to estimate the integration error used in a set of iterative integration calculations. When the estimated error is too large, the simulator switches to a smaller timestep. So reducing the value of RELTOL will improve accuracy, but obviously result in slower performance. Higher frequency elements in your circuit will require smaller timesteps and so may need a lower RELTOL setting.

Using a different technique to solve SPICE integration calculation options can sometimes help. Switching the "Method" from "Trapezoidal" to "Gear" is especially useful in resolving stability issues with circuits that have inductors and switching devices. However, when switching to the gear method, you should consider reducing RELTOL because these circuits often have higher frequency characteristics.

More information on resolving simulation problems can be found in the Multisim User Guide in the "Troubleshooting Transient Analysis" and "Troubleshooting DC Operating Point Analysis" sections. These sections are useful for other analyses as well, which often include a Transient or DC analysis. For example, a Fourier analysis operates by first running a transient analysis.

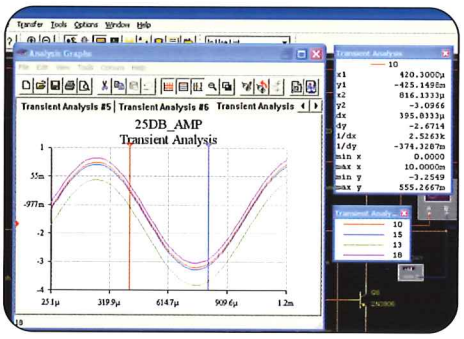


Figure 2 - Viewing multiple signals using the grapher.

OVERCOMING TWO-CHANNEL OSCILLOSCOPE LIMITATION

Many people want to use the oscilloscope to observe more than two channels simultaneously. To overcome the two-channel limit on the oscilloscope, you can use a transient analysis to display the same information. The oscilloscope is nothing more than a dressed up transient analysis that enables users to set the analysis with more familiar buttons and dials. The transient analysis can be a very powerful tool since it displays any and multiple nodal points in the circuit. Analysis results can also be exported easily, used in the post processor, or visually customized for printouts.

Tips & Tricks — ultiBOARD

By Frank Beltzner

TAKE CONTROL OF PART PLACEMENT

The "Part's" tab in Ultiboard's Design Toolbox is a very powerful feature for handling all the parts in your design. When a design is first imported from Multisim or Ultiboard, all parts need to be moved from their staft position outside the board outline to their final location within the board.

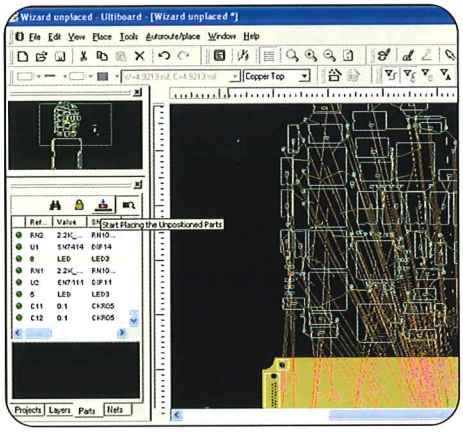


Figure 1 - Placing parts using the parts bin.

Simply hold the left mouse button over any part name in the part's tab list to drag that part onto the board. When you combine this with the ability to sort the parts in the list, you will speed up your part placement dramatically. Sort using any column property by clicking on the column header. If you then select the part sequencer button, every time you place a part, the next part on the list will automatically be attached to your cursor. Use the CTRL or SHIFT buttons to select multiple parts from the list.

To the left of each part in the list is a small circle indicating its status: light green if placed, dark green if unplaced, and orange if locked. You can also easily locate parts on the board by selecting the find button and the program automatically zooms in to the location on the board where the part resides.

IDEAS FOR SPEEDING UP PERFORMANCE

Ultiboard is the only program that truly operates in real time. Netlist updates are performed in true real time as you move your mouse around the board. This means that you get instant feedback no matter what you do. For example, you can place a part as close as possible to a track by nudging the part until you see the design rule violation appear, and then stop. In order to deliver this state-of-the-art real time feedback, Ultiboard is continuously updating the circuit's underlying netlist structure. On slower computers, or very large designs (especially those with large and many polygon areas), you may find the program begins to slow down. Here are some ways to speed things up.

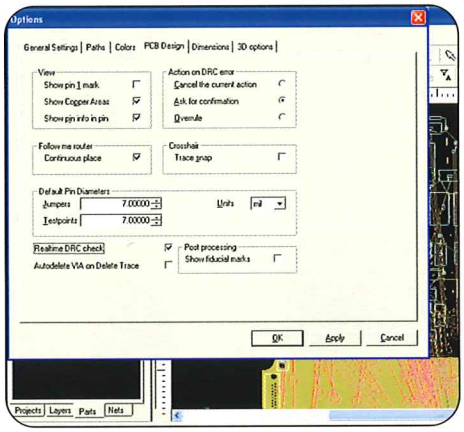


Figure 2 - Choosing DRC method.

First, make sure you are using Service Pack 2 which contains a number of speed enhancements. The next release after Service Pack 2 will contain even more optimization techniques that should eliminate the speed concern altogether. You can also try turning off realtime DRC (Tools > Options > PCB Design Tab). With this option off, there is no need to run batch checks. DRC will still be performed very frequently, running after you complete any action, but not as your mouse is moving during the course of the action. For example, when placing a part, you will see whether a violation occurs immediately after the part is moved, but not as you are moving. In the same dialog box, you can also turn off "Show copper areas". Finally, if you have design errors reported on your board, program performance will speed up once they are fixed. So don't ignore errors for long periods of time and try to resolve them as soon as possible.

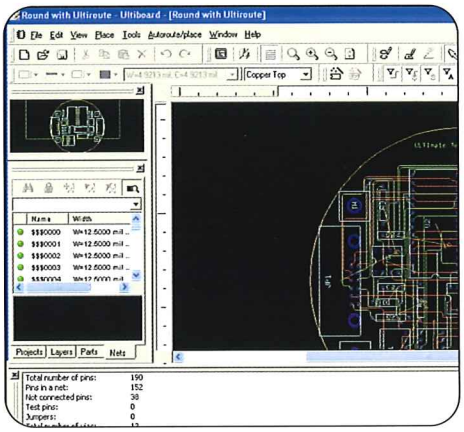


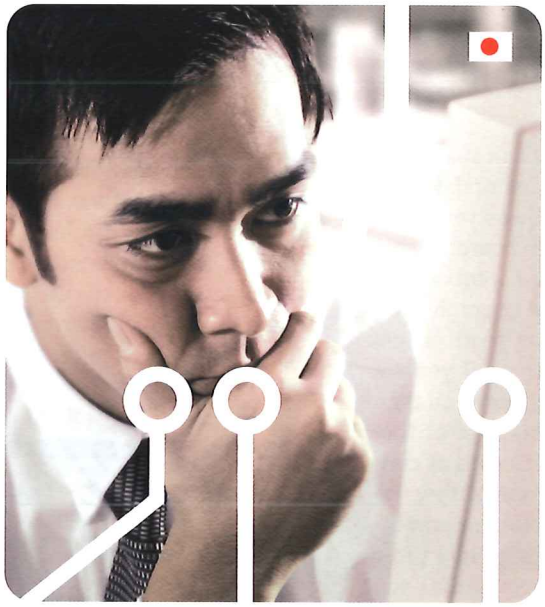
Figure 3 - Viewing board statistics.

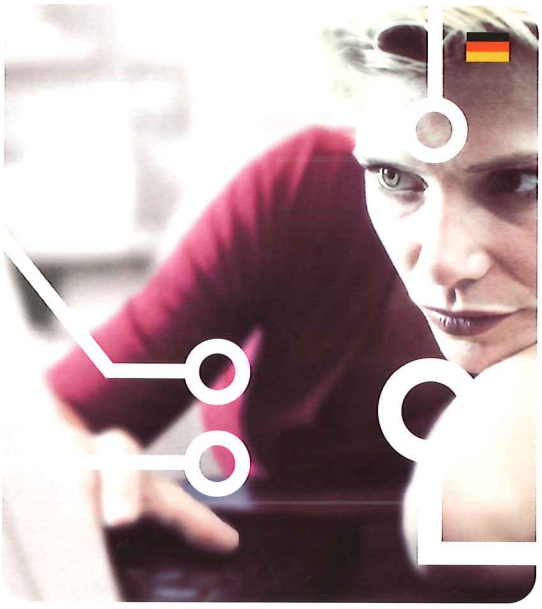
VIEWING COMPLETION

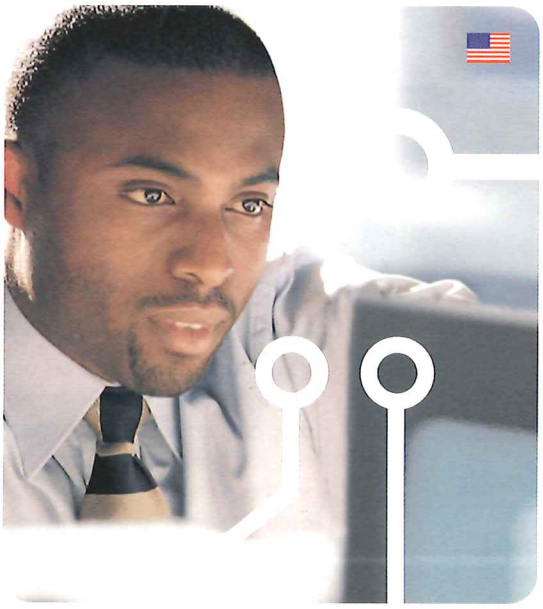
Please remember that an unrouted net is not a design error. Therefore, the design rule check and error output box will not tell you how much of your board remains uncompleted. To check completion, click on the "Status" tab of the outbox box and look for the "Completion" item which will tell you exactly what percentage of the nets are routed. If you see that the board is not complete, but cannot see which nets specifically need to be routed, use the "Nets" Design Toolbox. The color of the small circle next to each net name indicates whether that net is completed: bright green indicating it is complete, dark green means it is not. You can also locate the unconnected net by turning off all layers except the ratsnest layer. In that way you will immediately see the ratsnest for the unconnected net.

SOLVING EDA CHALLENGES AROUND THE WORLD.

Electronics WORKBENCH







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